DESIGN TECHNIQUES FOR RADIATION HARDENED PHASE-LOCKED LOOPS

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Abstract

Reliable operation of electronic equipment onboard the spacecraft requires radiation hardening. This article presents the design and analysis of a radiation hardened digital phase-locked loop. The effects of radiation both single event and total ionization dose on the phase-locked loops are briefly described. The constituent parts of digital phase-locked loops (DPLLs) are described and their impact on the overall radiation tolerance is reviewed. Single event hardening design techniques were additionally introduced into the digital PLL to improve its radiation performance. This PLL was fabricated in the Honeywell 0.35μm SOI CMOS process.

I. INTRODUCTION

Electronic devices employed on spacecraft have to be protected from the effects of radiation. Incorporating design techniques that mitigate the effects of radiation is called radiation hardening. Phase-locked loops (PLLs) are an important class of systems that are employed in a wide variety of applications. In order to design radiation hardened PLLs, the effects of radiation on these systems have to be studied. The investigation of the effects of radiation on test PLLs proves that the analog intensive design of a conventional chargepump based PLL is not suitable for radiation hardened applications. Fig. 1 shows the schematic of a conventional chargepump PLL. The analog blocks deteriorate as a result of total ionization dose. And single event effects cause loss of phase-lock during the operation. Digital blocks are inherently robust to the effects of radiation and a digitally intensive PLL would be ideal for radiation hardened applications. Well known digital radiation hardening techniques can also be incorporated into a digital PLL.

This article has been organized as follows. Section II describes the effects of radiation on phase-locked loops. Both total ionization dose and single event effects have been described. Section III describes the design of a digital phase-locked loop and the radiation hardening techniques are described in Section IV. Summary and conclusions follow in Section V.

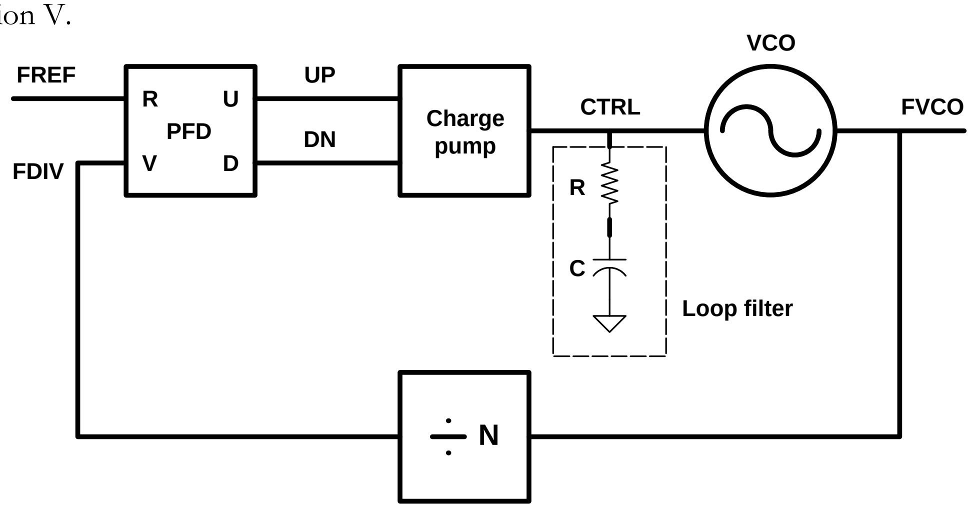


Fig. 1. Conventional analog intensive chargepump phase-locked loop.

II. EFFECTS OF RADIATION ON PHASE-LOCKED LOOPS

The effect of radiation on electronic circuits is twofold: (a) total-ionization dose (TID) and (b) single event effects (SEE).

A. Effects of Total-Ionization Dose: Total-ionization dose (TID) primarily produces a shift in the transistor threshold voltages. This transistor threshold voltage shift causes the PLL chargepump bias currents to change. The voltage-controlled oscillator frequency tuning characteristics are also shifted [1, 2, 3]. This shift in parameters causes the PLL loop parameters to change altering the PLL loop transfer function. This altered loop transfer function affects the loop acquisition behavior and closed-loop jitter performance.

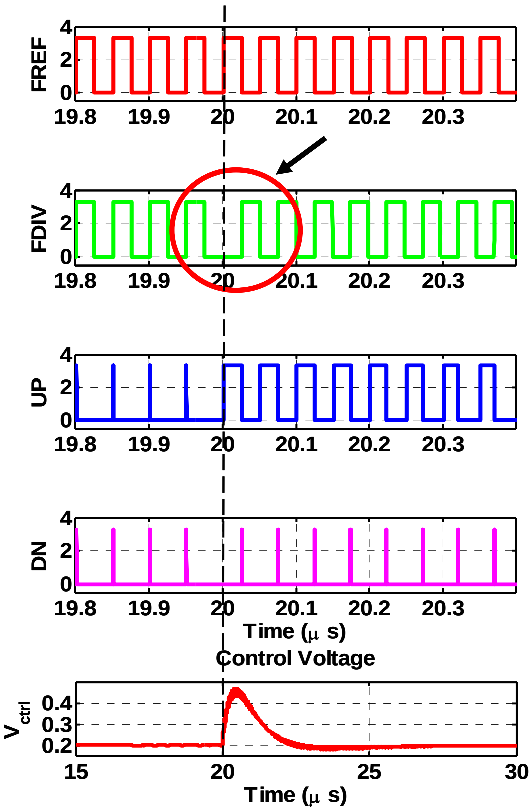


Fig. 2. A single event strike on the last stage of the frequency divider.

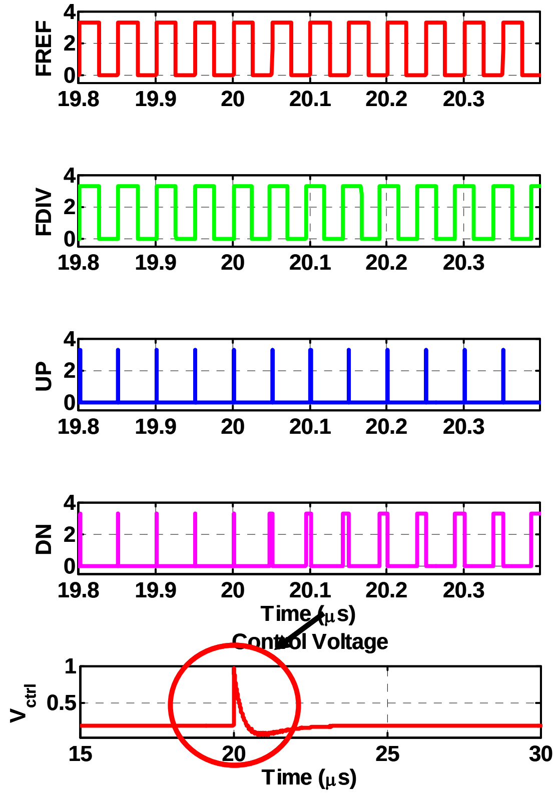


Fig. 3. A single event strike on the output of the chargepump loop-filter node.

B. Effects of single-event transients: Single-event transients (SET) are caused as a result of high energy particles striking an active device. During these transients, error currents are caused in the circuit. These error currents upset the node voltages and the stored digital values. Such errors are termed as single-event upsets (SEU). The last stages of the frequency divider, phase detector and loop filter are most sensitive to single event effects (SEE). A single-event strike on the last stage of the frequency divider or phase detector causes a huge phase error at the input of the PLL. This phase-error can cause the PLL to lose lock. The feedback around the PLL can restore lock eventually. But this would require several time-constants and the output of the PLL is rendered useless during this period. A single event strike on the output of the chargepump is the most hazardous of all. This would also cause the PLL to lose phase-lock. Figs. 2 and 3 show the effect of single events on frequency divider and the loop-filter. The frequency divider and phase detector can be made tolerant to SEE through incorporation of standard error prevention techniques such as triple voting. However, the output of the chargepump is an analog voltage and cannot be protected.

Unlike analog circuits, digital circuits are less susceptible to threshold voltage variations and can take larger doses of TID. Similarly, digital circuits can withstand larger error voltage transients. Hence, a digitally intensive phase locked loop is ideal for radiation hardening.

III. Design Of The Digital Phase-Locked Loop

Digital phase locked loops (DPLLs) have a number of advantages. The inherent digital nature makes them easy to design and implement. They are mostly composed of conventional digital logic gates. The loop-parameters of a digital phase locked loop can be controlled by modifying digital bits [4, 5]. Self-calibration can be implemented to counter the effects of TID. And redundancy can be built into the system to make it single event tolerant. Fig. 4 shows the schematic of a typical digital phase locked loop.

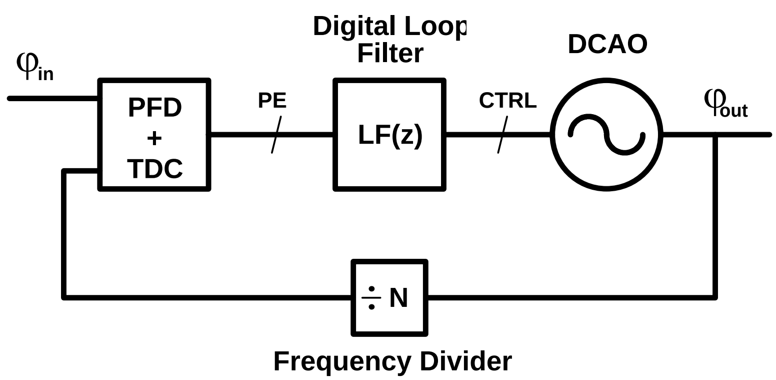


Fig. 4. Digital phase locked loop.

DPLLs have: (a) digitally controlled analog oscillator (DCAO), (b) frequency divider, (c) time-to-digital converter (TDC) and (d) digital loop filter (LF). The DCAO is an analog oscillator whose frequency is controlled by a digital word. The intrinsic oscillator can be an LC-tank or ring type architecture. Frequency tuning in an LC-tank oscillator is achieved by switching a parallel bank of capacitors. Similarly, a ring oscillator can be controlled by switching parallel current sources to control the tail current in the delay element. The output of the DCAO is divided to enable comparison with the input reference. The TDC compares the phases of the reference and the DCAO divided output to generate the phase error as a digital word. The LF filters the phase error to produce the control word for the DCAO.

(A) Digitally controlled analog oscillator: The DCAO is implemented as a three stage differential ring oscillator. The differential delay elements are Lee/Kim [6] type with dual control inputs, which allow for fine and coarse tuning. The schematic of the delay element is shown in Fig. 5. Two banks of current mirrors allow digital control of the fine and coarse tuning voltages. The tuning circuits convert the two 6-bit words into the analog V_{COARSE} and V_{FINE} voltages. The schematic of the fine tuning circuit is shown in Fig. 6. The coarse tuning circuit is identical. The operation is as follows: The digital input, $DF_{[0-N]}$, determines which current sources are drawing current from PM1. This sets the voltage at V_{FINE} and controls the speed of the oscillator. The resistor, R1, determines the unit value of current to be mirrored on the right half of the circuit. This resistor is off-chip to allow control of the trade-off between gain, resolution and tuning range.

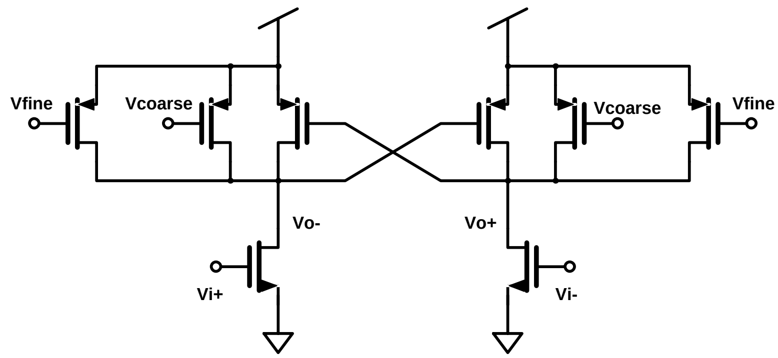


Fig. 5. Lee/Kim differential delay cell with dual tuning inputs.

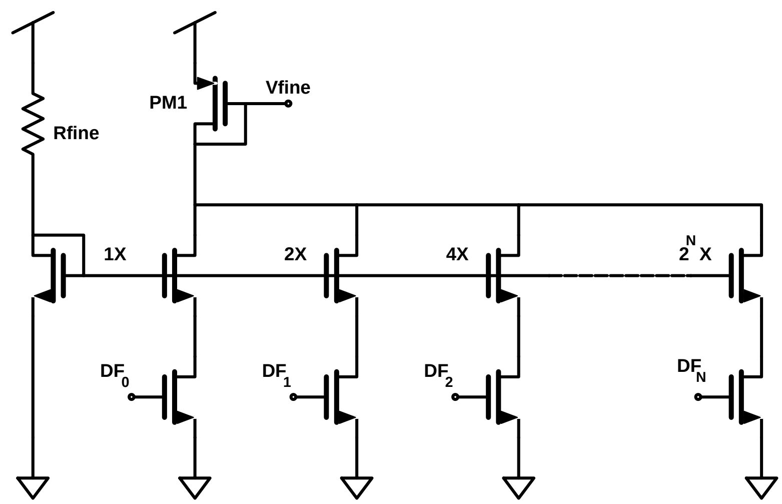


Fig. 6. Fine tuning control circuit.

(B) Frequency divider: The frequency divider is implemented as a cascade of divide-by-two stages. Each stage is a *true single phase clock* logic flip-flop [7] in feedback. A circuit diagram of the flip-flop and a single divide-by-two stage is shown in Fig. 7. The output of the displayed stage toggles at every rising edge of the clock. Hence, the output frequency is half that of the input frequency. Higher frequency division ratios can be achieved by cascading such stages. In order to make the division ratio programmable, a multiplexer has been added to enable us to select from a choice of division ratios. The schematic diagram of the programmable frequency divider is shown in Fig. 8. The possible division ratios are 8, 16, 32 and 64. They can be selected using the control bits **DIV1** and **DIV0**.

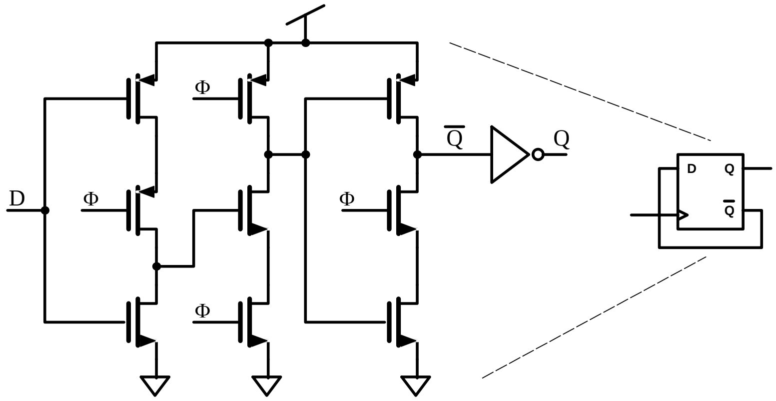


Fig. 7. TSPC flip-flop and a divide-by-two stage.

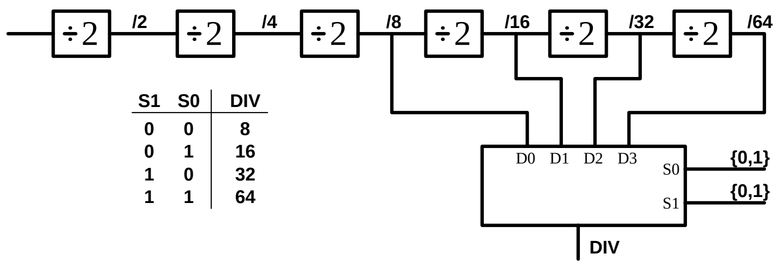


Fig. 8. Programmable frequency divider.

(C) Time-to-digital converter: The time-to-digital converter compares the input reference clock and oscillator divided output and generates the phase difference word. The operation is performed as follows. The phase/frequency detector (PFD) at the input of the TDC generates UP & DN pulses. A digital OR gate generates a pulse whose width is equal to the width of the wider of the two pulses. The delay chain in a TDC generates delayed versions of the OR pulse. When these delayed versions are latched by the falling edge of the OR pulse, the number of latch outputs that are high is the width of the OR pulse in number of inverter delays. A matching delay circuit is implemented using current starved inverters to compensate for the finite width of the UP/DN pulses in a PFD. A linear delay chain would require a large number of inverters and latches to cover the entire range. But an exponential delay chain would cover wider range with fewer stages. The initial stages of the exponential delay chain would have minimum possible delays to provide finer resolution and the subsequent stages would have larger delays to cover a wider range.

The minimum delay is the resolution of the TDC. It is denoted by **dT** and is about 80-100ps in the given process. This delay includes the effects of the loading of the subsequent stages and the latch. The value of the delay elements in the delay chain are dT, dT, dT, 4dT, 8dT, 16dT, 32dT, 64dT and 128dT. These nine stages cover a delay range of dT-256dT. The sign of the phase error is evaluated by latching the DN pulse with the UP pulse. The output would be high (sign is negative) when the DN pulse comes before the UP pulse. This occurs when the oscillator divided output leads the reference clock. The possible output values of the TDC are -256 to 256 in conjunction with the sign bit. The latch outputs are converted to 10-bit 2's complement signed digital word through the pseudo-thermometer encoder. Due to the exponential nature of the delay chain, the design of the encoder is greatly simplified. Fig. 9 shows the schematic of the TDC and the operation of the TDC is shown in Fig. 10.

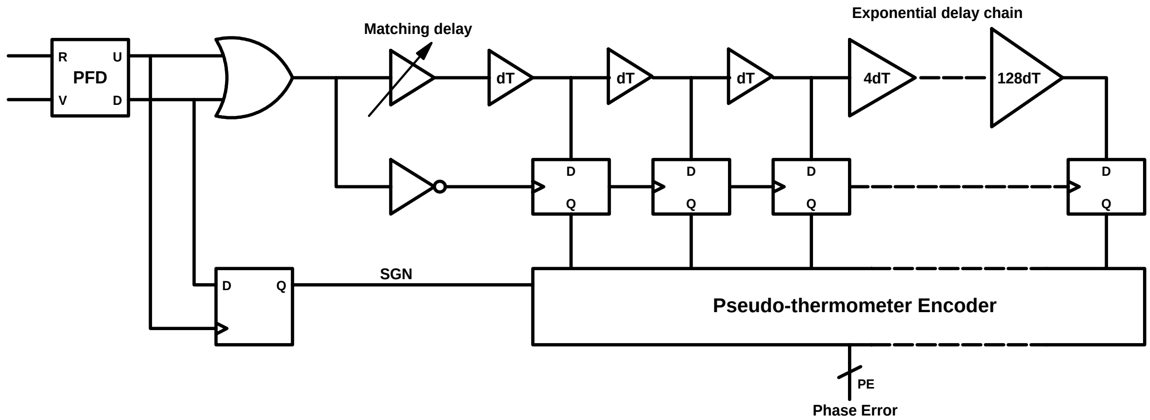


Fig. 9. Time-to-digital converter.

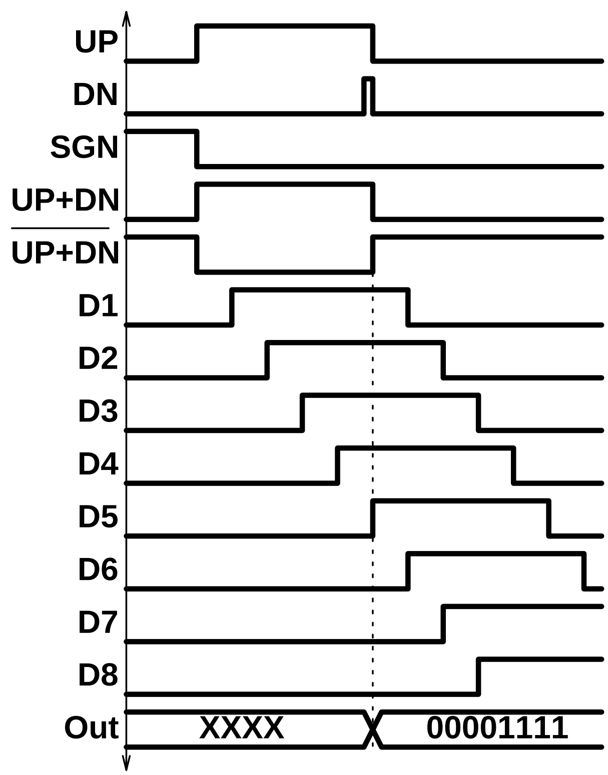


Fig. 10. Operation of time-to-digital converter.

(D) Digital proportional-integral controller: The loop-filter in the digital PLL is a proportional-integral controller. It has a proportional path and an integral path. The proportional path is analogous to the resistor in a chargepump PLL. Similarly, the integral path is proportional to the capacitor. Fig. 11 shows the architecture of the loop-filter. The integral path consists of an accumulator and a gain "β". The proportional path has a gain "α". The outputs of the proportional path and integral path are added and normalized to give the control word. The length of the accumulator register is 16-bits. This accumulator is implemented by stacking 16 single-bit accumulators. A schematic showing the single-bit accumulator is shown in Fig. 12. Implementing the proportional and integral gains would require digital multipliers. However, multiplication by powers of two can be achieved by adding zeros at the end of the word or truncating bits. Proportional gain is set to one and integral gain was set to 2^{-5}. To keep the jitter arising from the discrete nature of digital PLL low, normalizing gain has to be less than 1 and has been set to 0.5. Fig. 13 shows the implementation of these gains in the digital PLL.

The accumulator and the adder in the loop filter can overflow and give erroneous outputs. This can be prevented by implementing saturating adders. Overflow occurs when the inputs are positive and the output is negative. Similarly, underflow occurs when the inputs are negative and the output is positive. Error cannot occur when the inputs have opposite signs. The saturating adder detects overflow or underflow and limits it to the highest (2^N-1) or lowest (-2^N) values.

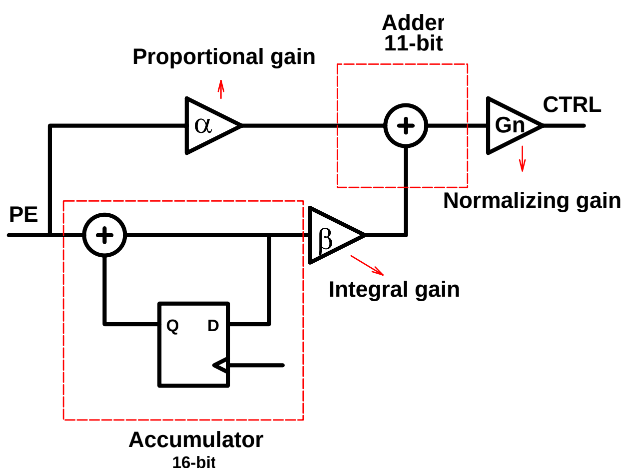


Fig. 11. Proportional-integral controller loop filter.

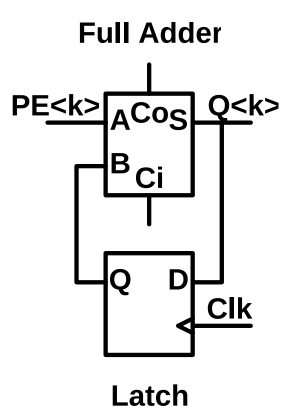


Fig. 12. One-bit accumulator.

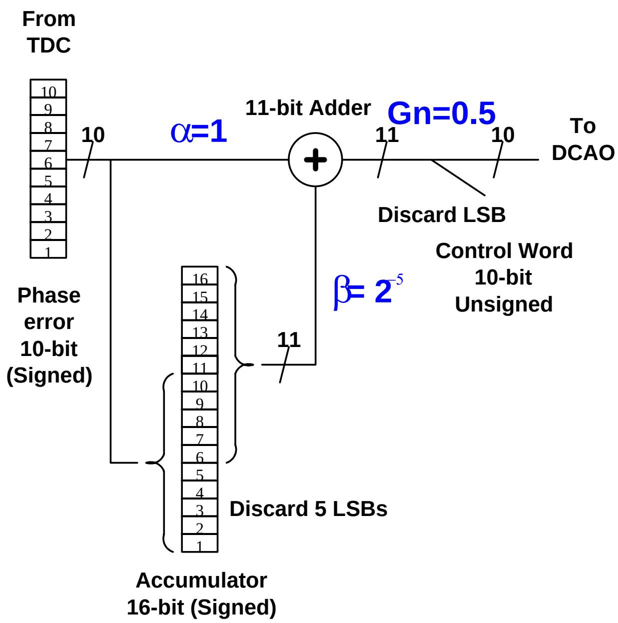


Fig. 13. Digital PLL controller.

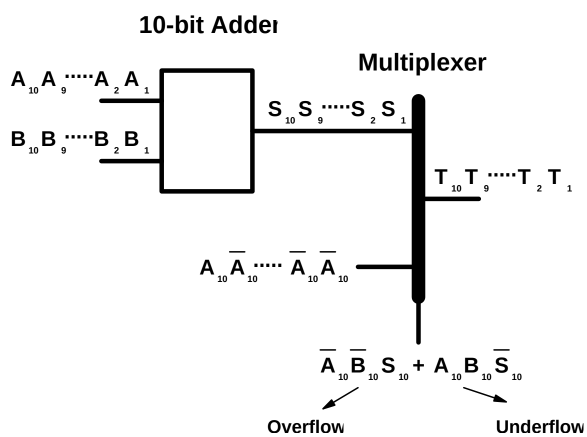
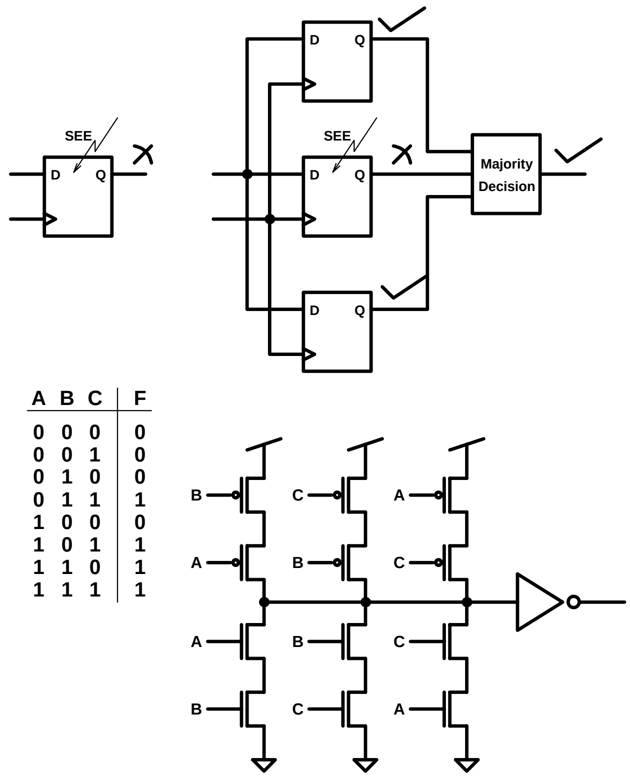


Fig. 14. Saturating adder.

IV. Radiation Hardening Of Digital PLL

Digital circuits are inherently robust to single event hits. The amount of transient error voltage required to upset a digital bit is large. Single event strike on combinational circuits is less harmful. Such circuits are driven and their normal states are restored almost immediately. However, a hit on the latches can be permanent. The saved state of a digital latch can be altered by a single event strike. Redundancy and error correction mechanisms are readily available for digital circuits and are amenable for implementation.



A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Fig. 15. Majority decision circuit.

Fig. 15 shows the schematic of a majority decision circuit. The figure shows that an error caused in a single latch cannot be prevented. However, if the latch is duplicated and a majority vote is implemented such an error can be prevented. Every latch which is susceptible to single event hit has to be replaced by the above block to make it single-event-tolerant.

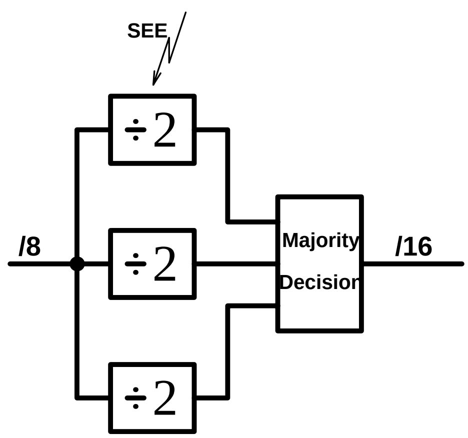


Fig. 16. SEE hardening of a frequency divider.

As described earlier, the last stages of the frequency divider, phase detector and the loop filter have sensitive digital values. These blocks have to be modified to make them single-event tolerant. A hit on the first three stages of the frequency divider causes phase errors less than one-eight of the reference cycle. However, these stages account for up to 80% of the power consumption in the frequency divider. Duplication of these blocks doubles the power consumption of the frequency divider. Hence, a trade-off has been made between the power consumption and the severity of the hit. In conclusion only the last three stages of the frequency divider have been made single event tolerant.

Similarly the PFD has also been made single event tolerant. Fig. 17 shows the duplication of the PFD. A bit flip on the MSBs of the TDC can cause an error transient. These bits can be secured by duplicating and implementing majority vote. Fig. 18 shows the new TDC with the MSB protected from SEE.

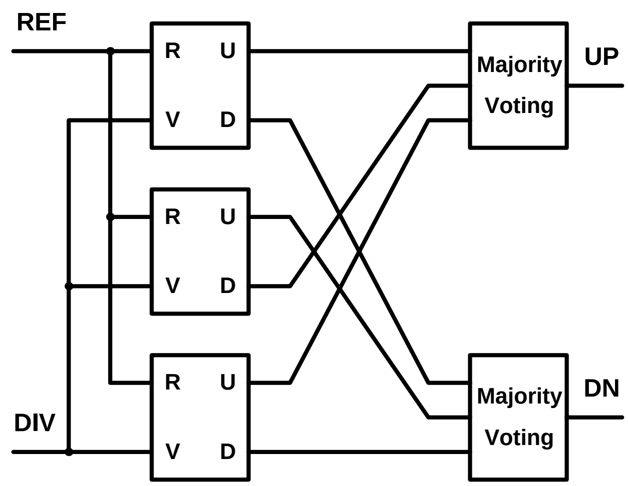


Fig. 17. PFD of the digital PLL protected using the triple voting scheme.

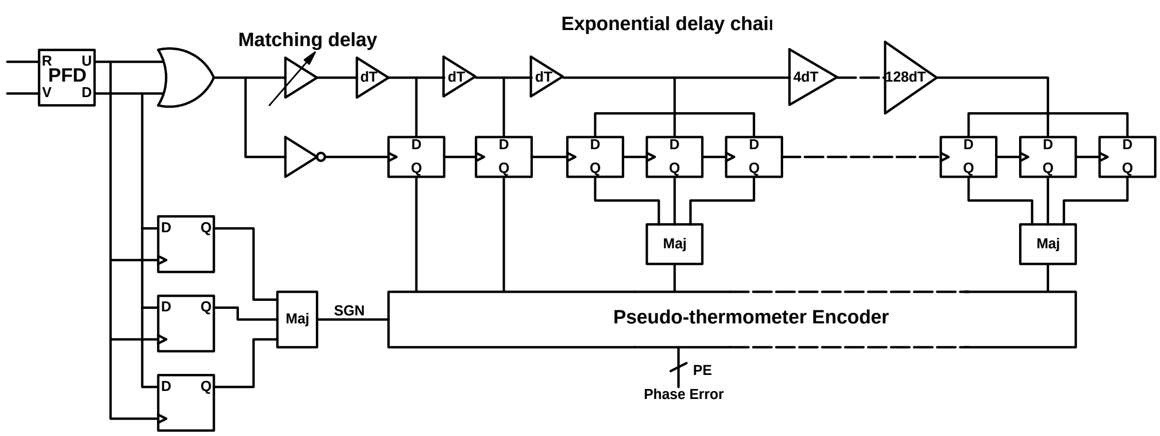


Fig. 18. TDC of the digital PLL protected using the triple voting scheme.

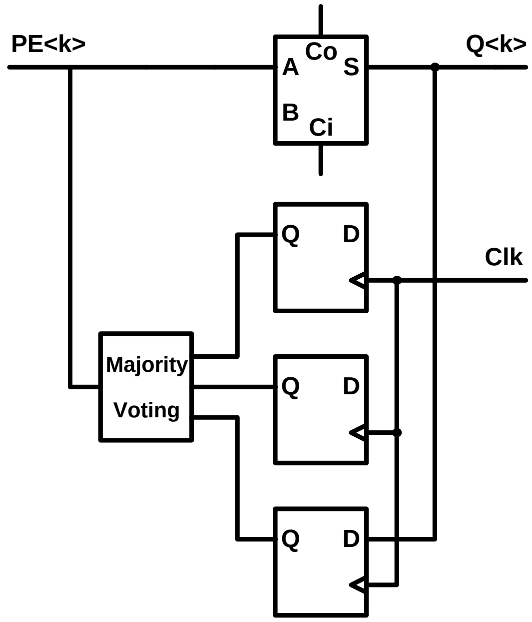


Fig. 19. Redundancy and majority voting scheme implemented on the accumulator.

Similarly, a bit flip on the accumulator can throw the PLL out of lock. The MSBs of the accumulator have also been secured. Fig. 19 shows the accumulator with redundancy implemented on the 10 MSBs of the accumulator.

V. SUMMARY AND CONCLUSION

A brief summary of the investigation of the effects of radiation on phase-locked loops was presented. This investigation revealed that the operation of a conventional chargepump based PLL in a single-event prone environment was unreliable. A strong argument for feasibility of implementation of digital PLLs which are immune to isolated single event hits was presented. The core digital PLL implemented to test these claims was described. Implementation of triple voting schemes on several blocks of the digital PLL that are prone to single-event hits has also been described. This digital PLL was fabricated in Honeywell 0.35μm SOI CMOS process.

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