Characterization of 1.2GHz Phase Locked Loops and Voltage Controlled Oscillators in a Total Dose Radiation Environment

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Abstract

Radiation hardness is an important consideration for Phase Locked Loops (PLLs) intended for space applications. Total dose radiation hardness of analog intensive circuits such as PLLs are of special interest as they do not lend themselves to calibration or redundancy techniques as readily as digital circuitry. This work summarizes measurement results obtained on a set of voltage controlled oscillators (VCOs) and a charge-pump PLL in a total dose radiation environment. The radiation was produced by a calibrated low energy X-ray (LEXR) source with dose rates of 300-500rad(SiO_2)/sec. The designs are completed in a 0.35um SOI process without specific design effort to reduce radiation effects. The circuits are all designed to operate nominally at 1.2GHz. They are characterized before and after irradiation with a total dose of 500kRad(SiO_2). The VCO's were measured for jitter and tuning range. The tuning range of the passively tuned LC-VCOs remained stable while the range of the actively tuned ring VCOs varied significantly. In addition, a more in depth test was done on the PLL. It was irradiated to 6.2MRad(SiO_2). The bias current as well as the tuning range were monitored throughout the test. The PLL was able to lock to a reference even after the 6.2MRad(SiO_2) dose. This paper describes the methodology and results of this testing and also presents insight on the design of high speed, rad-hard PLLs.

Introduction

Phase locked loops (PLLs) are versatile circuits used for many purposes. Their main feature is the ability to transform a low frequency reference signal to a higher frequency. This makes them appealing for clock generation and radio frequency transceiver circuits. PLLs have been studied extensively and are widely understood [1]-[8]. New variations on the basic charge-pump PLL (CPLL) shown in Figure 1 are an area of current research interest.

A CPLL works as follows: A reference signal (REF) is fed to a phase-frequency detector (PFD). The PFD compares the reference to its other input and outputs UP or DOWN pulses corresponding to which signal has a higher frequency. The charge pump (CP) interprets the UP and DOWN pulses and switches a current source to either add or remove charge from the loop filter (LF). The loop filter controls the dynamic behavior of the PLL. The output of the LF is the voltage controlled oscillator (VCO) control voltage. This is fed to the VCO which outputs a signal whose frequency is dependent on the VCO control voltage. The VCO output is optionally fed through a divider which divides the frequency of the signal by an integer N. This divided signal travels back to the second input of the PFD and is compared to the reference signal. When the phase and frequency of the reference and divided signals match, the PLL is said to be locked.

The divider allows the output of the VCO to operate exactly N times higher in frequency than the reference, but still track frequency changes in the reference or the VCO.
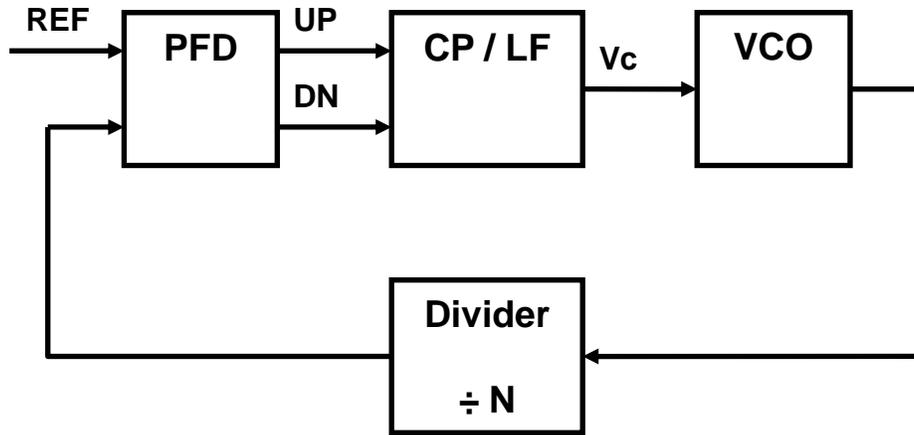
Figure 1. Block diagram of a CPLL.

Cosmic radiation [9] can interact with circuits in mysterious ways. The radiation effect is the interaction of radiation with the silicon crystal of a microelectronic circuit. They can be caused by several types of radiation which in turn can cause several different physical effects in silicon. Two effects are most commonly studied [10, 11]. The single event effect (SEE) is caused by a single energetic particle generating electrons and holes in the silicon which drift to nodes in the circuit. The total ionizing dose (TID) effect occurs when charge becomes trapped in the gate oxide of a transistor changing the characteristics of the transistor.   TID radiation is typically quantified by the rad unit of radiation energy absorption. One rad is equal to .01 Joules of energy absorbed per kg of material. The material must be specified for the unit to have meaning. Also note that Si and SiO_2 have different densities and 1 rad(Si) $\neq$ 1 rad(SiO_2). The first report of radiation interfering with circuits was in 1975 when a communications satellite detected 4 upsets (memory bits in error) over the course of 17 years [12, 13]. As technology dimensions scales to ever smaller values, the radiation problem has worsened. Now satellite electronics are always given thorough attention to the effect of radiation on the circuit. Research has been successful in determining the causes and several solutions to the radiation effect in digital circuits. Analog electronics, however, play a much smaller role in a satellite's electronic system and, therefore, have been somewhat neglected by the radiation electronics community.

The primary goal of this research was to explore new ways of mitigating radiation effects in PLL circuitry. A silicon on insulator (SOI) process seems especially suitable to this application. In an SOI process, the transistors are formed on a layer of silicon dioxide (SiO_2) instead of a thick layer of semiconducting bulk silicon. Thus, if an energetic ion were to strike an SOI transistor, only the electron-hole pairs above the SiO_2 would drift to nodes in the circuit. This could be an order of magnitude less that the charge collected in a traditional process [14].

Test Structures

Fourteen oscillators and two complete PLLs were designed for this project. Eight of the oscillators were ring type and six were LC oscillators. One of the PLLs used a ring oscillator and the other used an LC oscillator. The test structures were designed in the Honeywell MOI-5 process. This is an SOI process with a minimum gate length of 0.35 microns. Careful consideration was taken in the layout of the oscillators to maintain as much symmetry as possible between the differential parts of the circuit.

Four different versions of the Lee/Kim and Maneatis oscillators that were designed and analyzed in [15]-[17] were included on the test chip. These include a Lee/Kim oscillator with two different layout geometries, a Maneatis oscillator with transistors providing a symmetric load, and a Maneatis oscillator with a linear load as described in [16]. The two Lee/Kim geometries enable comparison of the traditional layout with asymmetric signal lines on delay cells to a new layout that matches signal delays at the expense of asymmetric power supply connections. [17] provides a detailed description of these ring oscillators. They are all three stage differential topologies.

The total chip area was roughly 5mm by 5mm. The test chip was packaged in a 121 pin ceramic pin grid array (PGA) package. The package has a taped on lid which can be removed to expose the bare die. Figure 2 shows a die photo of the test chip with the PLLs and VCOs highlighted.
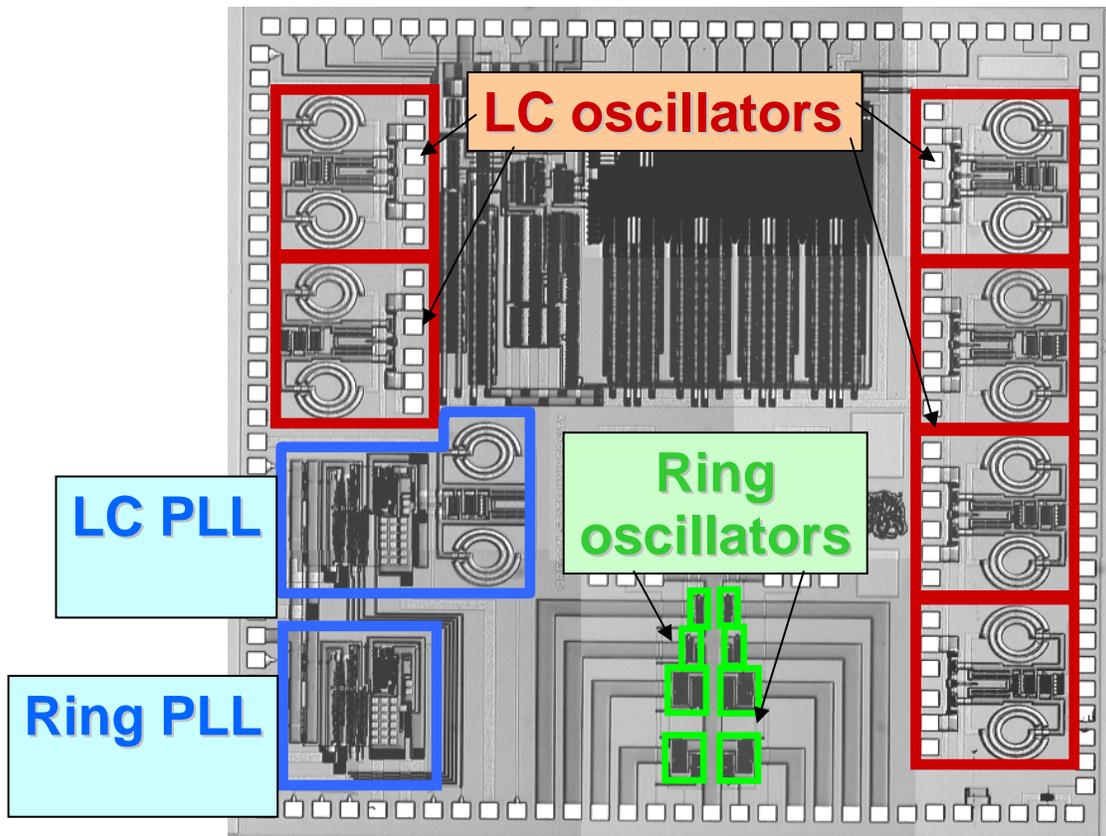
Figure 2. Die photo of first test chip.

Radiation Testing

The first test shuttle was exposed to total dose radiation at the Kirtland Air Force Base in Albuquerque, New Mexico, USA. Two tests were done. The first used a single 500krad (SiO$_2$) dose and measured all the oscillator test structures on the chip. The second exposed the chip to several doses and measured only the performance of the ring PLL. The LC PLL was unable to achieve lock preventing us from characterizing it. The Low Energy X-Ray (LEXR) source at AFRL provided the X-ray radiation for both tests. The measurements for the first test were done at OSU. The measurements for the ring PLL test were done on site at AFRL. The last data point of that test was taken after a delay at OSU to estimate the annealing effect in the Honeywell MOI5 process.

The radiation exposure was provided by the LEXR source inside a room with lead walls. The packaged chip was mounted on a circuit board which in turn was mounted in an aluminum box for mechanical stability and accurate positioning with reference to the LEXR source. This is critical for accurate dosimetry of the LEXR source.

The test board is designed to provide an interface for the input and output signals and also to provide bias to the test PLLs. The board was positioned such that only the active die was exposed to the radiation. The only active component on the test board is a voltage regulator

which sets the DC value of the VDD bus to 3.3V. The VDD bus is routed to all the different test structures and each is switchable with a jumper.   This allows us to monitor the current consumption of the PLL's and to only power up the structures of interest for the current test. The signal inputs and outputs are via SMA connectors.   The inputs and outputs were connected through 50-ohm connections to a digital storage oscilloscope. The cables were kept as short as possible, but they must pass through the walls of the LEXR chamber to reach the test equipment outside. Figure 3 shows a picture of the LEXR source in the test chamber. Attached is a cryo chamber which was not used in our test.

Figure 3. LEXR source in test chamber.

The lid of the ceramic chip package was removed during the test to expose the bare silicon die. This was to ensure that the X-ray radiation had an unimpeded path to the die.

Results – Single Shot

The first test was a single 500krad (SiO_2) at 100 rad/sec dose to all the oscillator test structures on the chip. Each oscillator's tuning range was measured before and after radiation. The 500krad had a small effect in some of the oscillators. It did not prevent any of the circuits from functioning. The most notable effect was the shift in the control voltage of the ring oscillators. The ring oscillators ran roughly 100MHz slower for a given control voltage after the radiation. The LC oscillators with no body ties also suffered from a shift, but in the opposite direction and on the order of a few tens of MHz. The tuning range was also compared to simulation data. Figures 4-9 show the tuning range of the VCOs.
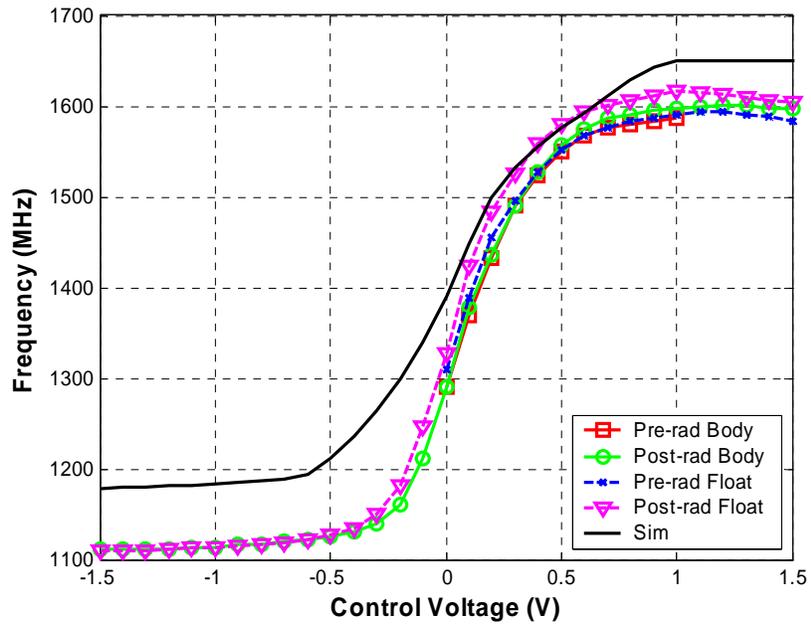
Figure 4. Tuning curve for PMOS source LC VCO.
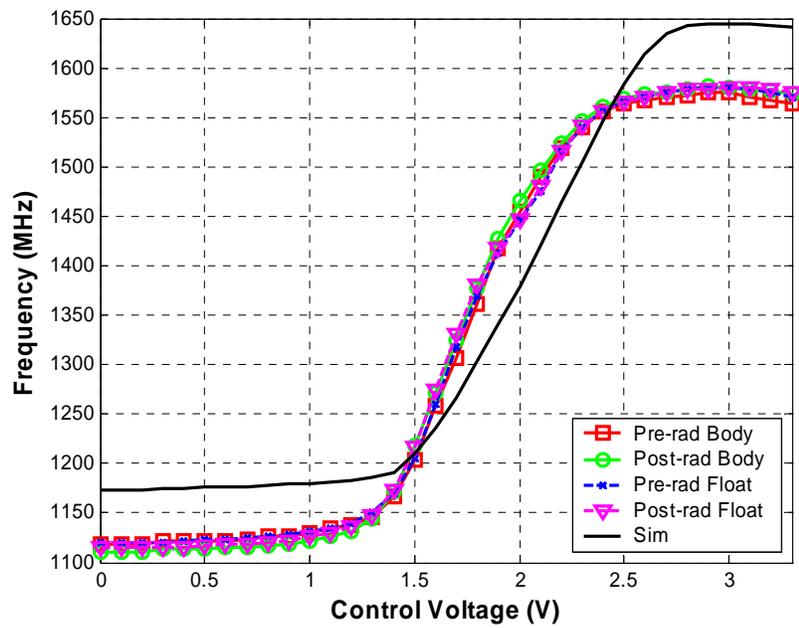
Figure 5. Tuning curve for NMOS source LC VCO.
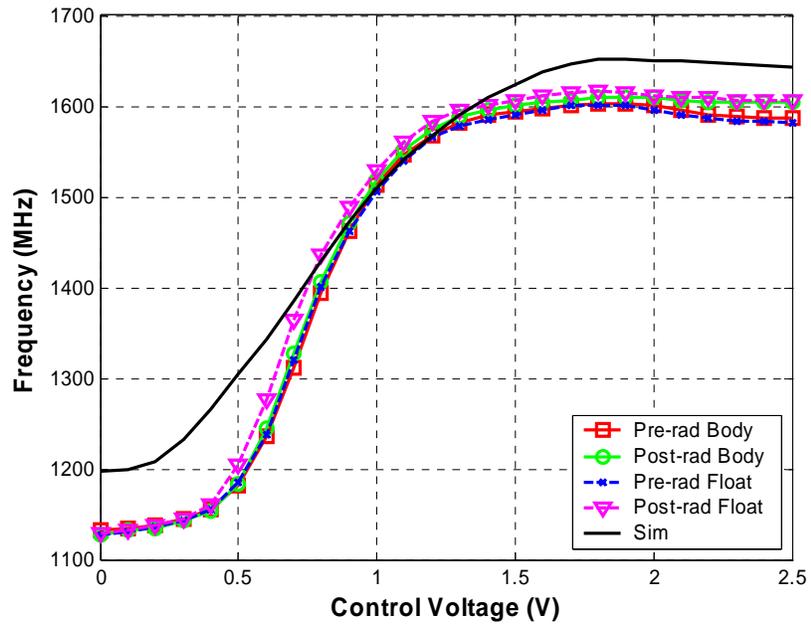
Figure 6. Tuning curve for complimentary source LC VCO.
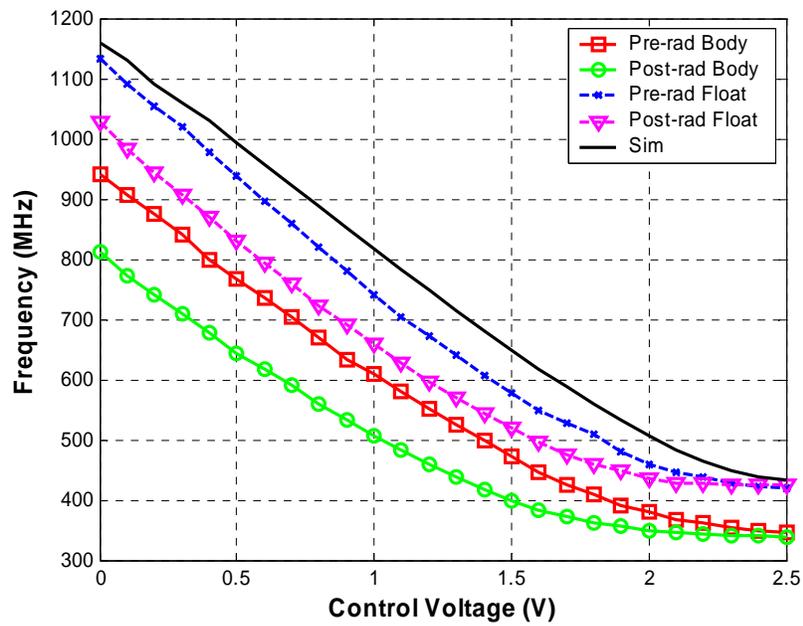
Figure 7. Tuning curve for Lee/Kim traditional layout VCO.
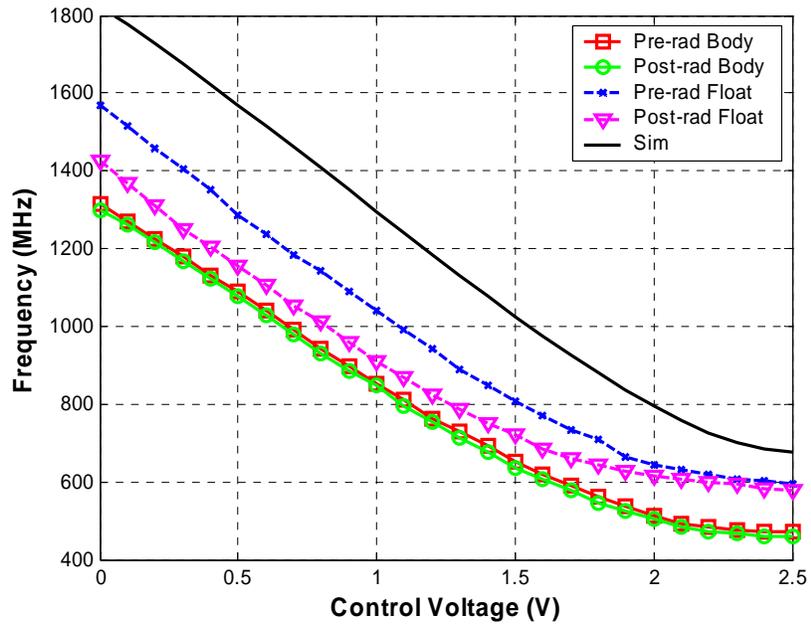
Figure 8. Tuning curve for Lee/Kim optimized layout VCO.
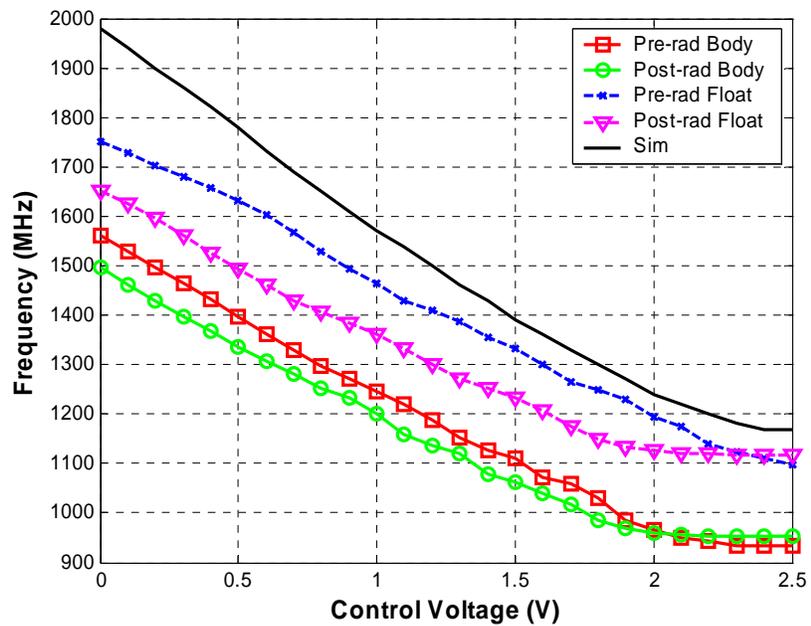
Figure 9. Tuning curve for linear-load Maneatis VCO.

Results – PLL Test

The ring PLL was tested for functionality at total dose radiation levels up to 6.2Mrad (SiO_2). The lock range was measured at 9 radiation levels and once again 35 days later with no additional radiation exposure. This final test was done to determine if annealing was contributing significantly to the measurements. Figure 10 shows the power consumption of the PLL as a function of the radiation dose. The measurement was taken at a reference frequency of 45MHz. After an annealing delay of 35 days, there is little change in the power consumption suggesting that the annealing effect is small.
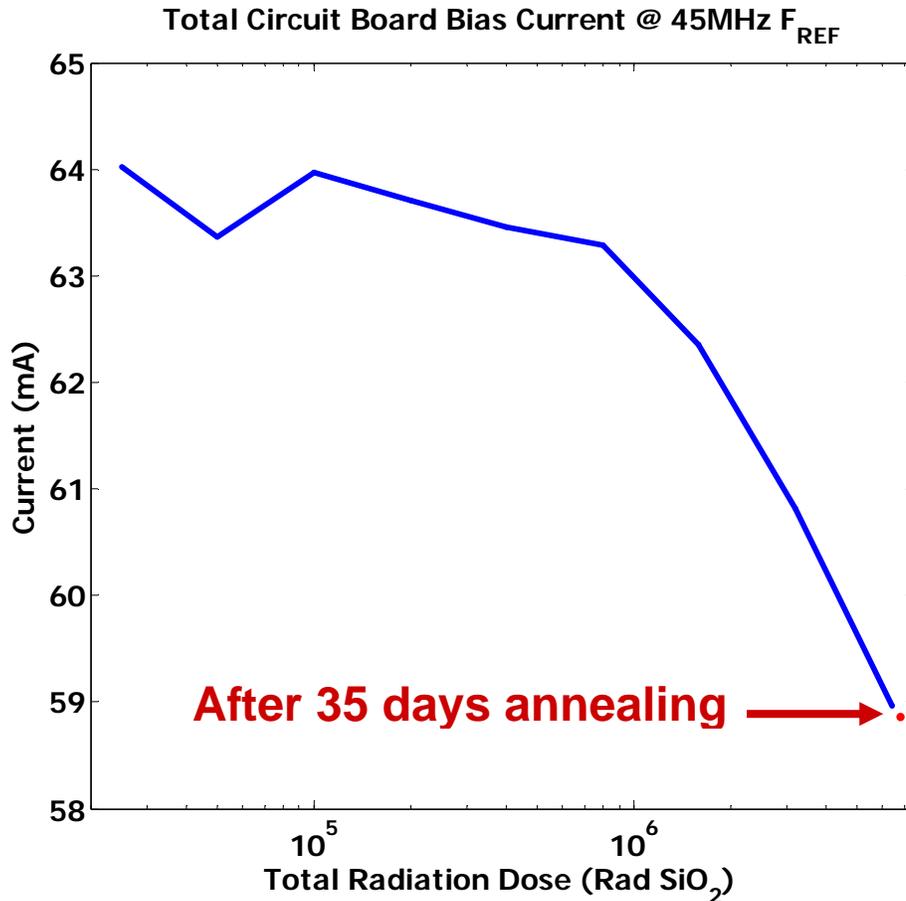
Figure 10. Power consumption of the PLL versus radiation exposure.

A plot of the lock range as a function of the total radiation dose is shown in Figure 11. The PLL was able to achieve lock even after the highest dose. The lock range was shifted somewhat from the radiation as can be seen in the plot. This effect would not prevent the PLL from operating properly. Again the final test was redone after 35 days to see the annealing effect.
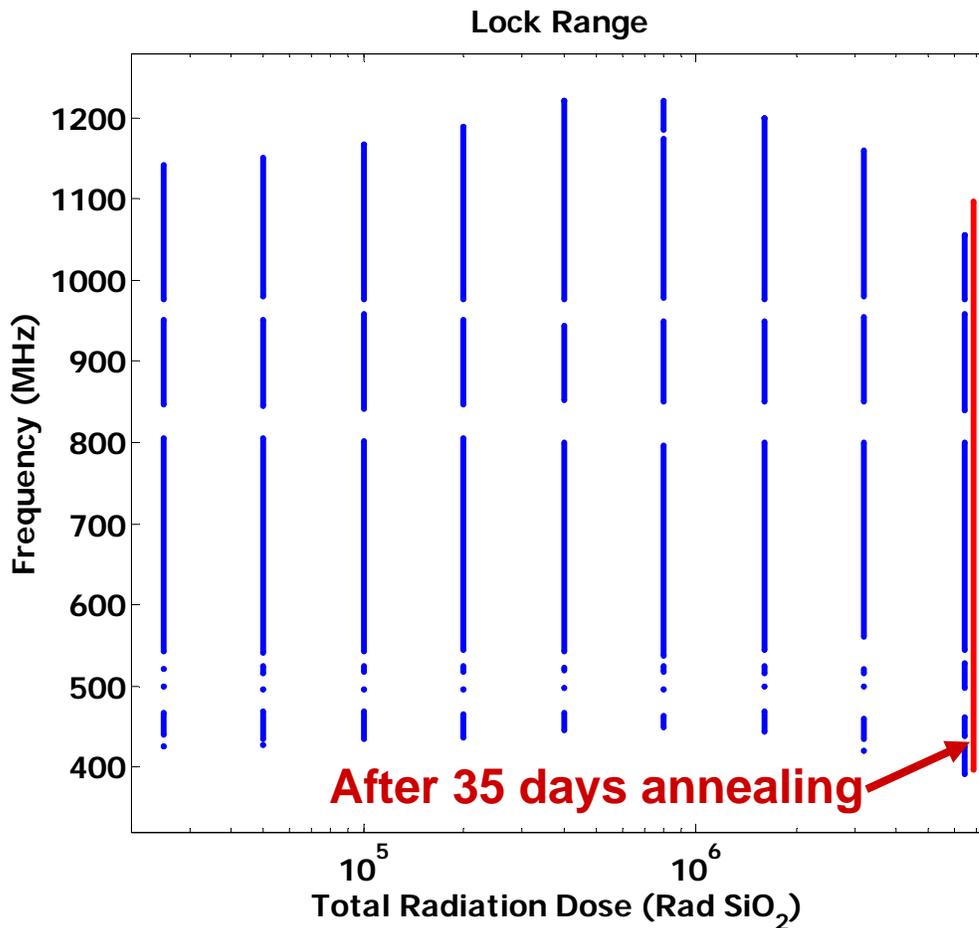
Figure 11. Lock range of the PLL versus radiation exposure.

There was a problem with the test setup at the AFRL that was preventing the PLL from achieving lock at some frequencies in the lock range. This is shown in the plot by the gaps in the lock range lines. We observed a large feedthrough of the oscillator output on the divided output. This was contributing to the problems achieving lock. The buffer for the VCO draws high currents from the power supply at a high speed. Using an improved test setup at OSU for the anneal test, the PLL was able to achieve lock throughout the lock range as expected.

When the test chip was designed, no on-chip bypass capacitors were used. This was done to have the ability of injecting power supply noise without the noise being filtered. We anticipated that the intrinsic capacitance of the metal traces and bondpads would be sufficient to keep the ripple off the supply lines. Silicon-on-Insulator processes, however, have much smaller parasitic capacitances than bulk processes because the metal layers are separated from the bulk by an insulator. The absence of bypass capacitors on the chip caused considerable power supply noise to exist. Although this did not prevent any of the blocks from functioning, it caused the performance of the blocks to deteriorate.

Simulations have been performed to estimate the effect of the package inductance with and without on-chip filter capacitors. A 4nH inductor was placed in series with the power supply of one of the Lee/Kim oscillators to model the bondwire. More complex bondwire and package models were simulated and the single inductor produced the most significant effect regardless of the rest of the model. Simulations were performed to examine the effect of on-chip capacitance on supply ripple. Figure 12 shows a schematic of the simulation setup. Simulation results for several values of on-chip capacitance are plotted in Figure 13. We can see that supply noise can be a big problem unless we have 10pF or more of on-chip decoupling. The second test chip benefits from this analysis.
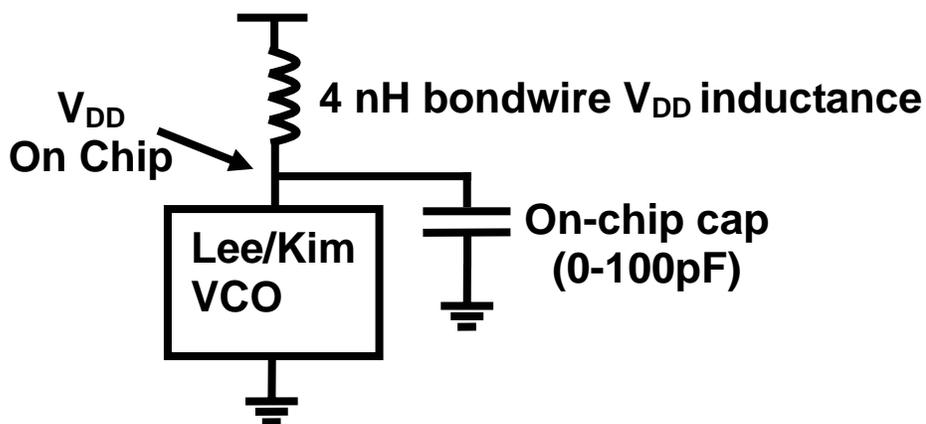
Figure 12. Schematic of power supply ripple simulation setup.
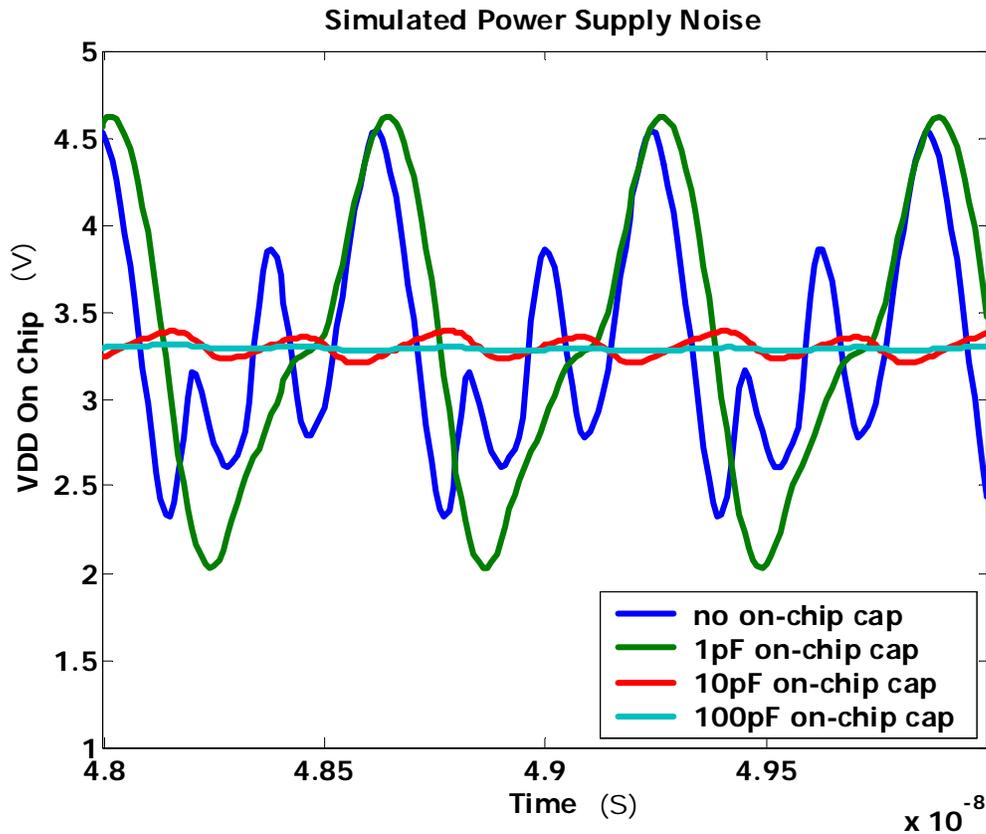
Figure 13. Simulation results for power supply ripple.

Conclusion

This paper gave details on the testing of phase locked loops for applications which will encounter radiation. A test chip was designed and fabricated in a 0.35μm SOI CMOS process. The test chip included two PLLs, 8 ring VCOs, 6 LC VCOs, and a number of other test structures. The tuning range of the VCOs was shifted due to the total dose radiation. The ring VCOs saw a much greater shift than the LC VCOs. The ring PLLs tuning range was also shifted from the radiation. It was able to achieve lock even after the highest dose of 6.2Mrad. The LC PLL was unable to lock in all the tests.

As space exploration and development matures, electronic systems of increasing complexity are required to power and control spacecraft. In addition, as silicon transistors scale to smaller and smaller sizes, the effects of radiation can become more and more pronounced. These two factors ensure that radiation tolerant electronics will require development long into the future.

Rising costs and complexity of state-of-the-art wafer fabrication facilities prevents the use of exotic, radiation hard processes. This guarantees that circuits will need to be designed to be radiation hard in standard processes. Future design techniques will likely include converting

as much of the circuit to the digital domain as possible. This allows mature mitigation techniques for digital circuits to be used.

Acknowledgment

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