A 1.4V 10b CMOS DC DAC in 0.01mm²

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Abstract

A low voltage 10-bit DC DAC is fabricated in a standard 0.18μm CMOS process. The DAC is optimized for circuit calibration in large ASICs and occupies 0.01034 mm² (110μm x 94μm) of die area. Creative layout and current mirroring techniques are implemented to minimize area while providing output current with sufficient headroom. The measured DNL/INL is better than 0.7/0.75 LSB and 0.8/2 LSB for 1.8V and 1.4V power supplies, respectively. The DAC consumes 3.96mW at 1.8V and 3.08mW at 1.4V.

Introduction

Digitally controlled and area efficient calibration circuits play an important role in the design of complex, mixed-signal ASICs. Because these calibration circuits are commonly used throughout the chip, their impact on the total chip design should be minimal. Two critical factors to consider when designing these circuits are the area and power consumption.

In high-speed circuits, the die area of a calibration circuit is critical. The high-speed blocks need to be placed close together to minimize parasitic loading. The area occupied by the calibration circuit should be minimized to avoid interfering with the high-speed circuitry. In addition, the calibration circuitry should be low power to minimize the total chip power. A compact low frequency digital-to-analog converter (DAC) is effective for these applications.

Design Considerations

A. Architecture

The proposed 10b CMOS DAC for DC operation has the segmented R-2R ladder architecture shown in Fig. 1. The 3 MSBs are thermometer coded, while the lower 6 bits are a straight R-2R ladder. A typical thermometer plus R-2R architecture (1) would include the 64x branch in the R-2R ladder, hence placing 2 resistors in the 64x branch and adding a resistor between the 32x and 64x branches. The proposed architecture has 2 resistors in parallel for each branch of the thermometer portion instead of one. This method is effective in eliminating linear process gradients by placing the MSB resistors in a common centroid scheme in the layout. The chosen architecture results in a good trade-off of static performance and area consumption.

B. Device Sizing

The effect of random mismatch errors on the required relative current source matching is often characterized with
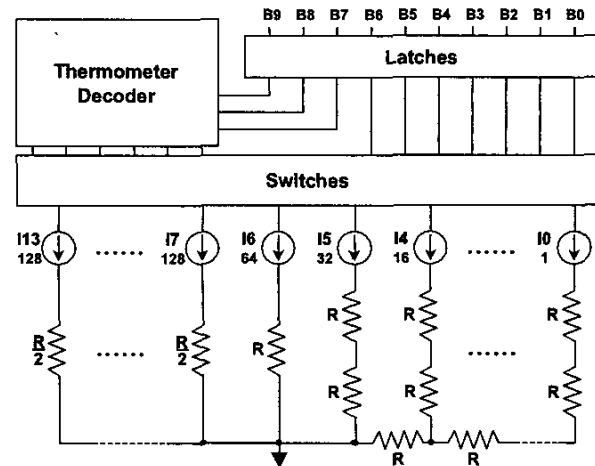

Fig. 1. The 10-bit segmented architecture

Monte Carlo simulation or a simplified set of equations (2). The results are used with closed form equations (3), (4) to determine the current source device dimensions.

Since the data available at the time of fabrication was insufficient, the effects of random mismatch errors and process gradients for the transistors and resistors were examined by mathematically modeling the DAC exactly as it appears in the layout. The parameters for the mathematical model were estimated by extrapolating the matching statistics of older CMOS processes.

The resulting dimensions of the unity current source device are W=0.52μm and L=0.36μm, and the width of the poly resistors is W=1.06μm. The digital portion of the DAC was implemented with minimum device geometry.

Implementation

The prototype IC is realized in standard 0.18μm CMOS. The 1024 unity current source devices are laid out in a pseudo common centroid scheme to reduce the effects of thermal and process gradients. The layout was studied extensively using a mathematical model that accounts for the location of each unit current source element and each unit resistor. Errors can be applied randomly or in a combination of horizontal and vertical gradients. The entire die area of the DAC, including the op-amps and power supply lines, is 0.01034 mm² (110μm x 94μm). Fig. 2 shows the die micrograph with the different areas labeled for clarity.
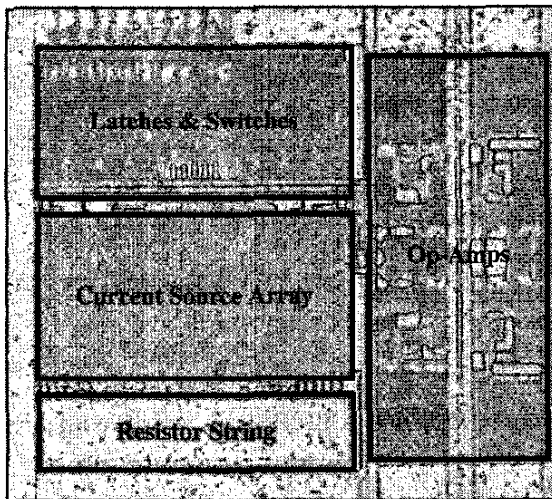
Fig. 2. Chip Micrograph

Fig. 3. Measured INL/DNL at 1.8V

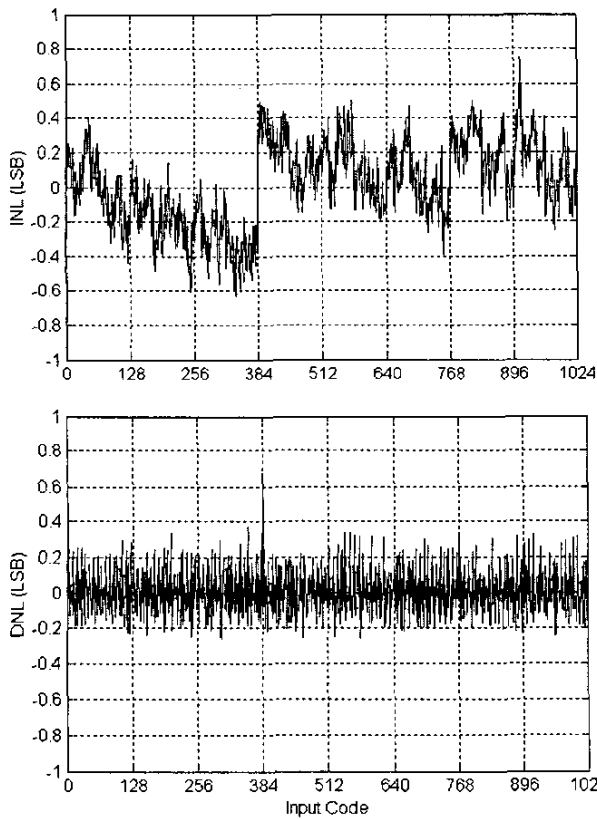

Fig. 4. Measured INL/DNL at 1.4V

Measured Results

Fig. 3 shows the measured integral non-linearity (INL) and differential non-linearity (DNL) with a 1.8V power supply, and Fig. 4 shows the measured INL and DNL with a 1.4V supply. In both cases the DAC is 10-bit monotonic, and bette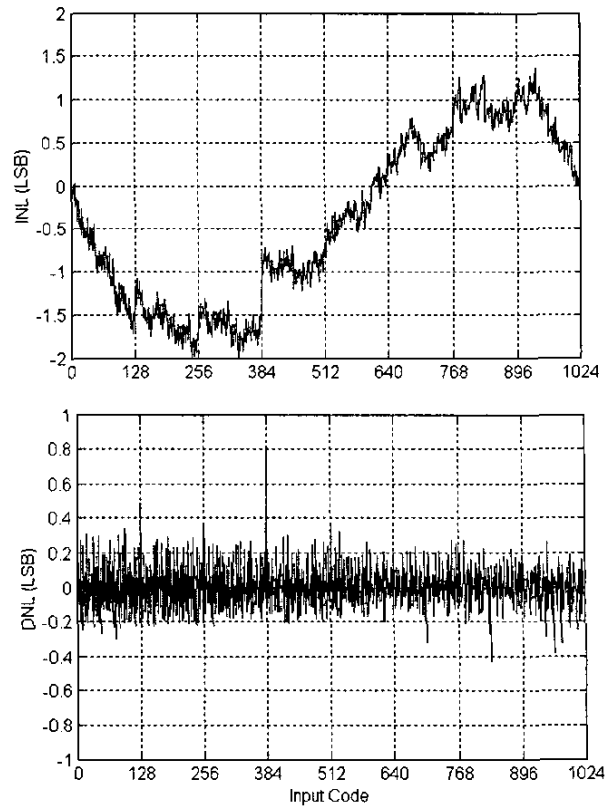r than 8-bit linear which complies with the most critical requirements. The IC consumes 2.2mA of current, independent of power supply voltage.

Conclusion

In this paper, the design and layout of a 1.4V, 10-bit DAC cell were presented. The DAC cell was designed with die area conservation, and 10-bit monotonicity being the primary goals. A fundamental tradeoff between system performance and layout area has been examined and implemented.

Measured results show that 10-bit monotonicity and better than 8-bit linearity are achieved at 1.4V. The DAC cell presented is ideal for applications where a small, low power, low frequency calibration DAC is needed for the plethora of trim adjustments in large mixed-signal ASICs.

References

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