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A Noise-shaping Accelerometer Interface Circuit for Two-chip Implementation*

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This paper introduces a new architecture for sensor interface circuits using a delta–sigma modulator. The three-level force feedback allows the use of a digital compensator to stabilize the loop. A 3rd-order delta–sigma structure shapes the op-amp noise and allows a two-chip implementation with high loop gain at low frequencies.

Keywords: Sensor; Delta–sigma; Interface; Force feedback; Mismatch shaping; Acceleration

INTRODUCTION

Modern micromachining technology allows the fabrication of mechanical sensors on chip. A successful application is the accelerometer, widely used in automobile air-bag systems. This is basically a capacitive sensor, but its capacitance is quite small. There are several ways to sense the capacitance accurately. Our previous result [1] shows that one can use the sensor as the input capacitor in the delta–sigma loop. The other solution using the delta–sigma loop is based on force feedback [2,3]. For the accelerometer, force feedback is attractive, since it offers the potential of wide dynamic range [4].

In this paper, we introduce a two-chip implementation of a capacitive sensor interface circuit, intended especially for the accelerometer. There are several advantages to fabricating the circuits separately. First, one can use this circuit technique when there is no access to micromachining technologies, and a commercial sensor must be used. Second, it is likely to provide higher yield since the micromachining process is still complicated and failure-prone. Third, one can use more advanced process for the interface circuit and use more transistors, because micromachining usually uses older processes. One can also apply this circuit for multiplexed sensors. Once a two-chip solution is obtained, it will be less challenging to generate a single-chip implementation.

To implement the interface circuit separately, we have to solve two problems arising from stray capacitance due to the wiring between sensors and circuits: large *kTC* charges and large gain for the op-amp noise. A cross-coupled integrator is proposed to solve these problems. Also, using a higher-order delta–sigma loop increases the loop gain and reduces nonlinearity.

In the second section, we describe the sensor characteristics. In the third section, we propose a new noise-shaping structure with higher loop gain and three-level force feedback. In the fourth section, we show how the noise from the op-amp will be shaped by the additional integrator. The simulation of the additional stage with compensator is described in the fifth section. Our conclusions are given in the sixth section.

ACCELEROMETER SENSOR

Figure 1 shows the model of the accelerometer used in the simulation and design of the interface circuit. It consists of two capacitors with a common center plate.

The top and bottom plates in Fig. 1 are fixed, but the center plate will move when there is acceleration. This movement creates the capacitance changes. By detecting the capacitance changes, we can measure the acceleration. The dynamic characteristic of the sensor can be modeled by

$$H(s) = \frac{x(s)}{\alpha(s)} = \frac{1}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \tag{1}$$

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(a) $C_{S1} = C_{S2}$ (b) $C_{S1} > C_{S2}$

FIGURE 1 Accelerometer sensor (C_{S1}, C_{S2}: sensor capacitors, C_{FF1}, C_{FF2}: force-feedback capacitors).

where x is the mass displacement, α is the acceleration, $\omega_n = \sqrt{K/M}$ is the resonant frequency, $Q = \sqrt{KM}/D$ is the quality factor, K is the spring constant, D is the damping factor, and M is the mass of the center plate.

With recent micromachining technology, this type of sensor can be fabricated in a small size and has a potential use in many applications. However, the necessary detection of small variation of the capacitance is challenging. Typical sensor capacitance is 100 fF, its variation is only ~0.1 fF, and it may have to be detected with a resolution of the order of 1 aF (10^{-18} F).

INTERFACE STRUCTURE

Figure 2 shows the proposed structure for the sensor interface circuit. An integrator is added for additional noise shaping to get a higher SNR at low frequencies, and to filter the op-amp noise, amplified due to the large parasitic capacitance between the chips, as discussed in the "Noise limitations" section. Extra compensation is needed, because the sensor itself has the second-order characteristic as given in Eq. (1), and the system would be unstable without a compensator due to the excessive loop phase shift. One possible solution is to insert an analog compensator before the quantizer [3]. This implementation is not suitable for the third-order structure, because the effect of the last stage will be canceled by the local loop. Hence, the position of the compensator was chosen as shown in Fig. 2. Now the input of the compensator is a digital signal, and hence the compensator can be realized as a simple digital differentiator with a transfer function $(1 - z^{-1})$.

Figure 3 shows the root loci and the magnitude responses of the quantization noise transfer function for various quantizer gains. As the root loci verify, the digital compensator stabilizes the loop for all values of the quantizer gain.

Circuit Realization

Figure 4 shows the proposed circuits. The first stage is on the sensor chip and the second stage is on the interface circuit chip.

At the input stage of the interface chip, an integrator is used, instead of an amplifier as in Ref. [3]. This is because here we have amplified op-amp noise, since there are large parasitic capacitances. Due to the input integration, the input-referred op-amp noise will be shaped in the proposed circuit, as discussed later in the "Noise limitations" section. The interstage nodes are not switched to the ground, and this is a major difference from ordinary integrators. Since these nodes are not switched, the *kTC* charge noise from the large parasitic capacitances does not enter the signal. The sensor capacitors are switched in a cross-coupled connection. This scheme doubles the amplitude of the sensor signals, and also reduces the large common-mode signal.

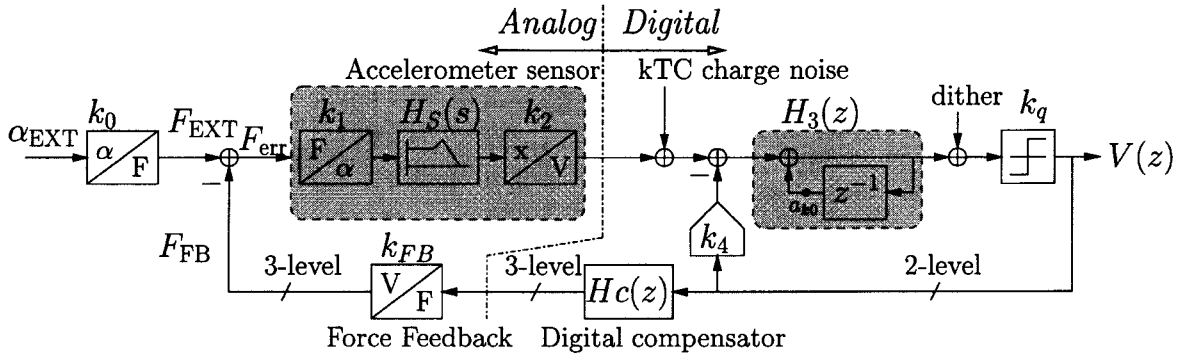


FIGURE 2 Third order sensor circuit block.

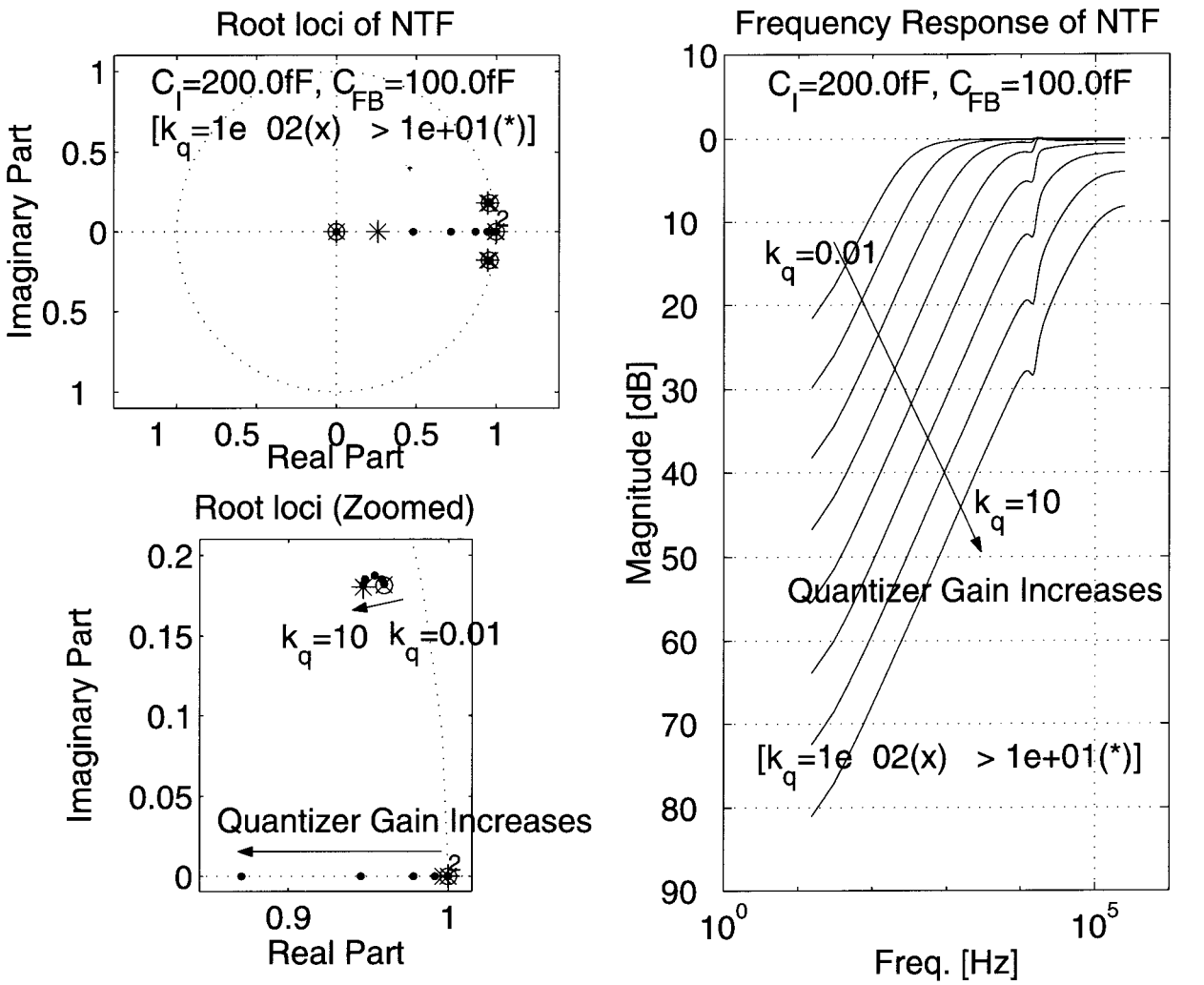


FIGURE 3 Root locus and noise transfer function (NTF).

C_{FB1} and C_{FB2} provide two-level electrical feedback from the quantizer to the integrating stage. The digital compensator creates a zero to stabilize the loop and provides a three-level output since the quantizer is a two-level one. The three-level force feedback is applied to the sensor capacitors. Unlike the complex analog compensator needed in Ref. [3], a simple digital compensator is adequate to stabilize the system. The challenge here is the three-level feedback signal generated from the output of the digital compensator. This three-level signal has to be very accurate and highly linear.

Three-level Force Feedback

Figure 5 shows the proposed force-feedback arrangement. V_1 and V_2 are the voltages at the top plate and the bottom plate, respectively. V_{cm} is the center plate voltage. d_1 and d_2 are the distances between the plates of the capacitive sensor, C_{S1} and C_{S2}, respectively. Here $d_1 + d_2 =$ constant, because the outer plates of the sensor capacitor do not move. Typical values of d_1 and d_2 are around 1 μm. x is the displacement due to the acceleration.

There is nonlinearity in the force feedback in terms of the mismatch between d_1 and d_2, and the displacement x. This nonlinearity problem can be solved using a time-averaged force-feedback scheme during the $\phi 3$ and $\phi 4$ phases as shown in Figs. 4 and 5.

In Fig. 5(a), let the potential of the center plate be 1 V. If $d_1 < d_2$ after applying acceleration, the top plate will be connected to $+2.0$ V, and the bottom plate to -2.0 V during both $\phi 3$ and $\phi 4$ phases for moving the center plate in the same direction. This creates higher electric field in the bottom capacitor, and pulls down the center plate towards the middle.

If the center plate moves down and it causes $d_1 > d_2$ in Fig. 5(b), the voltages of the outer plates will be reversed, causing the center plate to move up.

If the digital compensator's output is zero ($y_M = 1$), the force feedback is averaged in time using the $\phi 3$ and $\phi 4$ phases. This will be done by applying the force feedback in the opposite direction during $\phi 3$ and $\phi 4$. This approach is similar to that proposed for a three-level DAC in Ref. [5].

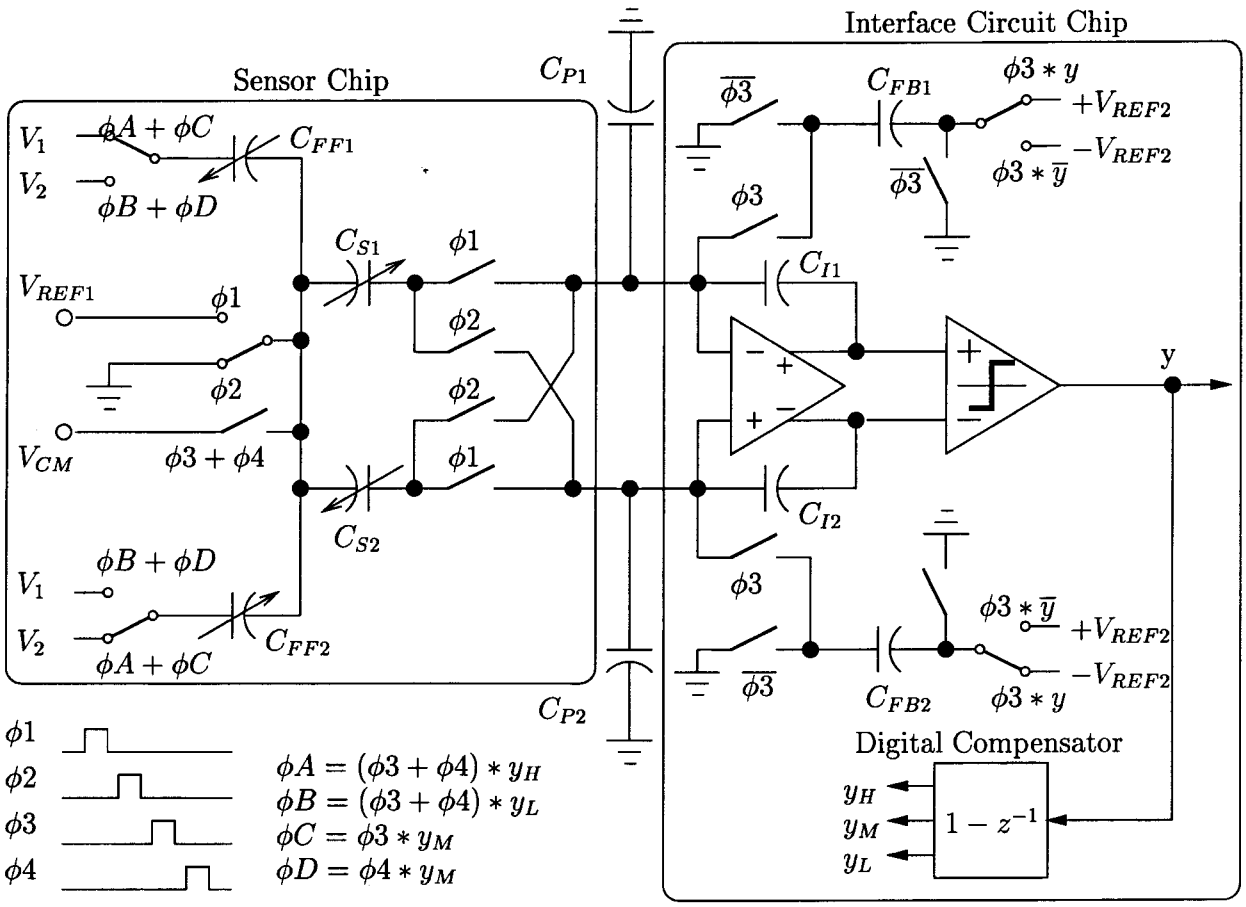


FIGURE 4 The two-chip accelerometer.

Hence, the feedback force F_{FB} has three levels, given by

$$F_{FB} = \begin{cases} F_{FB+} = -\frac{\epsilon A}{2}\left[\left(\frac{V_1 - V_{cm}}{d_1 + x}\right)^2 - \left(\frac{V_{cm} - V_2}{d_2 - x}\right)^2\right] \\ \quad \text{if } y_H = 1 \\ (F_{FB+} + F_{FB-})/2 \\ \quad \text{if } y_M = 1 \\ F_{FB-} = -\frac{\epsilon A}{2}\left[\left(\frac{V_{cm} - V_2}{d_1 + x}\right)^2 - \left(\frac{V_1 - V_{cm}}{d_2 - x}\right)^2\right] \\ \quad \text{if } y_L = 1 \end{cases} \tag{2}$$

where y_H, y_M, and y_L are the outputs of the digital compensator. The signal y_H is activated when the compensator output is $+2$, y_M is active for 0, and y_L is for -2, since the digital compensator outputs are $+2$, 0, -2. The voltages used for the outer plates, V_1 and V_2, do not need to have exactly the same absolute values.

Table I shows how to select the three-level force feedback during the $\phi 3$ and $\phi 4$ phases. The sign " + " or " − " shows the direction of the force feedback. First-order mismatch shaping can be expected when $\phi 3$ and $\phi 4$ are chosen alternatively, as indicated in Table I. This is a significant advantage for the three-level DAC because it assures high linearity.

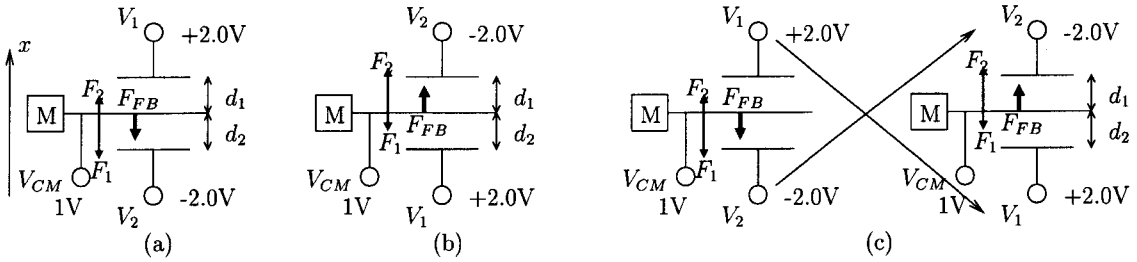


FIGURE 5 Time-averaged force-feedback scheme: (a) $y_H = 1$, (b) $y_L = 1$, (c) $y_M = 1$.

TABLE I Force-feedback direction

Comp. Output	$\phi 3$	$\phi 4$	
$y_H = 1$	+	+	
$y_L = 1$	−	−	
$y_M = 1$	+	−	alternated
	−	+	

NOISE LIMITATIONS

The comparison between an amplifier and an integrator is next performed, for the circuits of Fig. 6. The standard integrator and amplifier have parasitic capacitors at the input node. Also, both have the noise sources $v_n(t)$, which are modeled as the input-referred noise of the op-amp.

Output Noise

The output voltages for the amplifier and the integrator can be found in the z domain analysis, assuming the op-amp gain is very high.

For the amplifier,

$$V_{\text{o,amp}}(z) = \frac{C_s}{C_f} V_{\text{in}}(z) + \frac{C_s + C_p + C_f}{C_f} V_n(z) \qquad (3)$$

Equation (3) shows that the input-referred noise of the op-amp is amplified more when there is a large parasitic capacitor C_p, and that the output noise will be independent of frequency.

For the integrator, the output voltage with the parasitic capacitor C_p is given by

$$V_{\text{o,int}}(z) = \frac{C_s/C_f}{1 - z^{-1}} [V_{\text{in}}(z) - V_n(z)] + \frac{C_p + C_f}{C_f} V_n(z) \qquad (4)$$

The first term in Eq. (4) shows that the noise will be integrated with the gain of C_s/C_f, which is the same as the signal gain. Note that this integrated noise is *independent* of the parasitic capacitor. The second term in Eq. (4) shows that the op-amp noise will also be amplified due to the large parasitic capacitor C_p.

Input-referred Noise

Now the input-referred noise is considered in order to compare the signal to the noise explicitly. The input-referred noise of the amplifier $V_{\text{ni, amp}}$ and the integrator $V_{\text{ni, int}}$ are given by Eqs. (5) and (6), respectively:

$$V_{\text{ni,amp}}(z) = \left(1 + \frac{C_p + C_f}{C_s}\right) V_n(z) \qquad (5)$$

$$V_{\text{ni,int}}(z) = \left(1 + \frac{C_p + C_f}{C_s}(1 - z^{-1})\right) V_n(z) \qquad (6)$$

Equation (5) shows that the input-referred noise is the result of the amplified op-amp noise. If the parasitic capacitor C_p is large, the input-referred noise is also large. Equation (6) shows that the amplified noise due to the parasitic capacitor will be first-order shaped. Thus, at low frequencies, higher SNR can be expected using the integrator than using the amplifier.

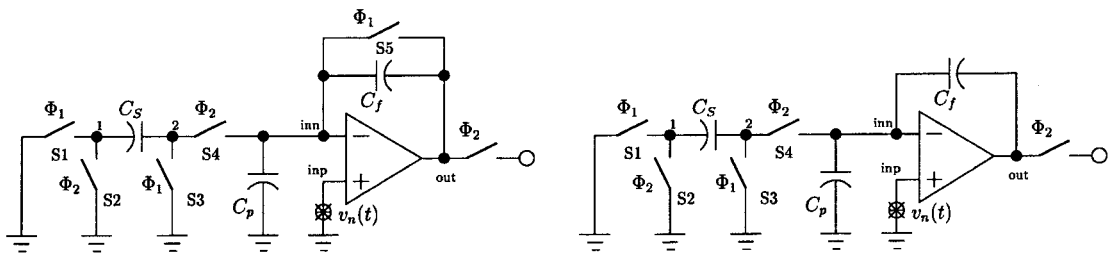
SIMULATION RESULTS

The proposed two-chip system was simulated using MATLAB under the conditions $\omega_n = 15$ kHz and $Q = 4$, with a sine-wave acceleration input 5 G (49.05 m/s^2) peak. Due to the additional stage, it provided good noise shaping at lower frequencies and hence yielded a high SNR.

The sensor structure was based on the lateral fringe capacitors with small mismatch. According to Ref. [3], the mismatch is about 0.02%. We also assumed a 0.02% mismatch in the sensor capacitors. The simulation results are shown in Fig. 7. There is a dc component due to the mismatch in the displacement, but no visible harmonics.

CONCLUSIONS

A two-chip implementation was proposed for an accelerometer. The first stage of the sensor interface circuit is an integrator, which is preferable to an amplifier from a noise point of view. The spectrum of the amplified op-amp noise due to the parasitic capacitors is then shaped. The additional integrator increases the loop gain



(a) Amplifier (b) Integrator

FIGURE 6 The circuits for noise comparison.

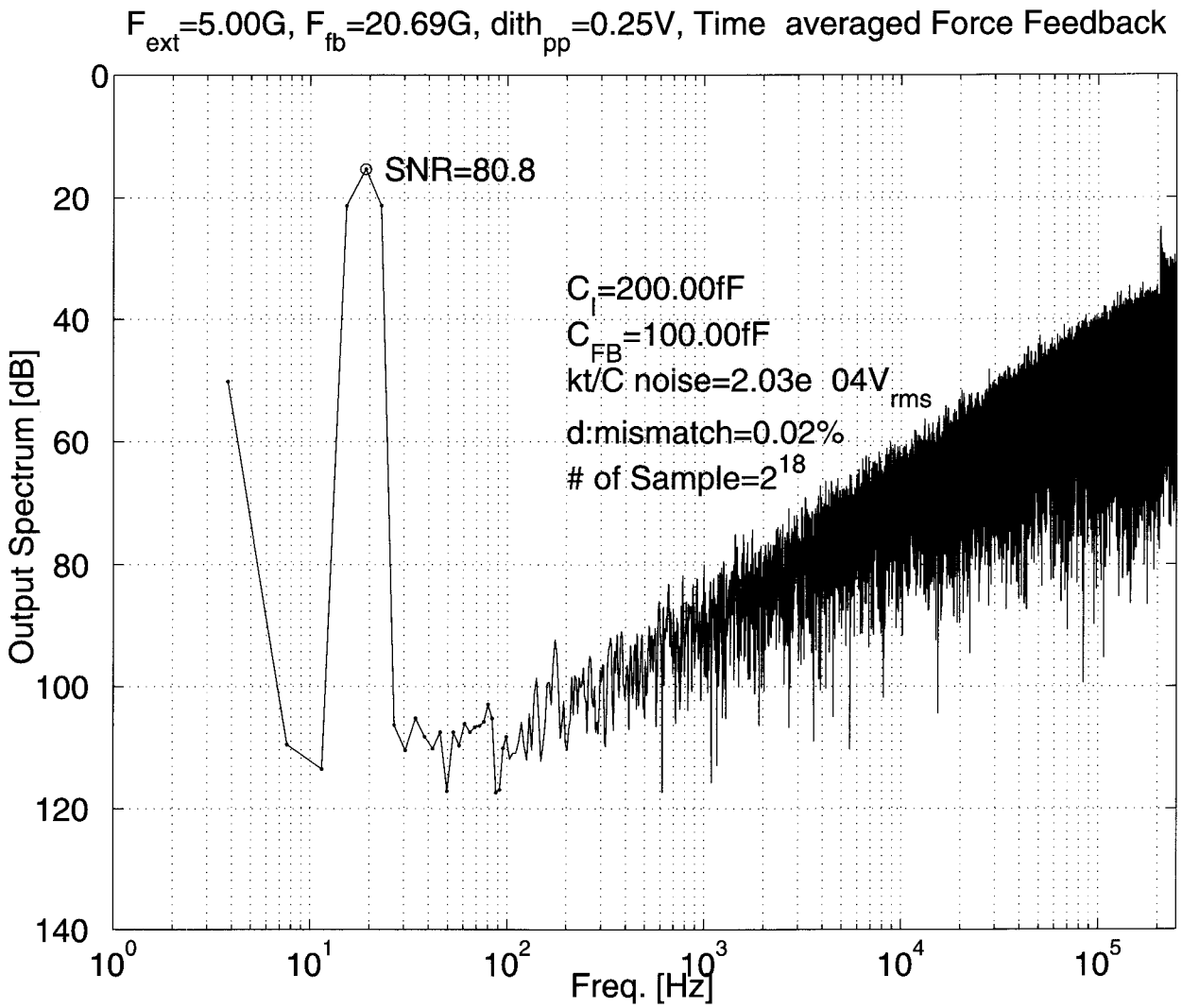


FIGURE 7 Output spectrum with sine-wave input, a 0.02% mismatch between sensors.

and reduces the harmonics. To make the loop stable, a new architecture was chosen for the delta–sigma modulator with digital compensation and three-level force feedback. This interface circuit technique is applicable not only to accelerometers but also to capacitive sensors requiring two-chip implementations.

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References

[1] Wang, B., Kajita, T., Sun, T. and Temes, G.C. (1997) "High-accuracy circuits for on-chip capacitor ratio testing and sensor readout", *Proc. IEEE Instr. Meas. Conf.* **2**, 1169–1172.

[2] Henrion, W., DiSanza, L., Ip, M., Terry, S. and Jerman, H. (1990) "Wide-dynamic range direct digital accelerometer". In: *Tech. Dig. Solid-State Sensors and Actuators Workshop*, SC, (Hilton Head Island), pp. 153–156.

[3] Lemkin, M. and Boser, B.E. (1999) "A three-axis micromachined accelerometer with a CMOS position–sense interface and digital offset-trim electronics", *IEEE J. Solid-State Circuits* **34**, 456–468.

[4] Yazdi, N., Ayazi, F. and Najafi, K. (1998) "Micromachined inertial sensors", *Proc. IEEE* **86**, 1640–1659.

[5] Wang, X., Qin, W. and Ling, X. (2000) "Cascaded parallel oversampling sigma–delta modulators", *IEEE Trans. Circuit Syst.* II, **47**, 156–161.

Authors' Biographies

Tetsuya Kajita received the BS degree and MS degree from Waseda University, Tokyo, Japan, in 1988 and 1990, respectively. He joined Yamatake-Honeywell Co, Ltd, Kanagawa, Japan, in 1990, and has worked at Solid State Advance Center as an analog ASIC design engineer. From 1993 to 1994, he was a visiting scholar at Electrical and Computer Engineering Department, Oregon State University. He is taking a sabbatical leave from Yamatake-Honeywell (now Yamatake Corporation

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Gábor C. Temes received the Dipl Ing from the Technical University of Budapest in 1952, the Dipl Phys from Eötvös University, Budapest in 1954 and the PhD degree in Electrical Engineering from the University of Ottawa in 1961. He held academic positions at the Technical University of Budapest, at Stanford University and at UCLA. He is now Professor at Oregon State University (OSU). He served as Department Head at both UCLA and OSU. He is co-editor and co-author of several books, including Analog MOS Integrated Circuits for Signal Processing (Wiley, 1986) and Delta–Sigma Data Converters (IEEE Press, 1997). His recent research has dealt with CMOS analog integrated circuits, as well as data converters and integrated sensor interfaces.