

0.9V 12mW 2MSPS Algorithmic ADC with 81dB SFDR

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Abstract—An ultra low-voltage CMOS two-stage algorithmic ADC incorporating background digital calibration is presented. The adopted low-voltage circuit technique achieves high-accuracy high-speed clocking without the use of clock boosting or bootstrapping. A resistor-based input sampling branch demonstrates high linearity and inherent low-voltage operation. The proposed background calibration accounts for capacitor mismatches and finite opamp gain error in the MDAC stages via a novel digital correlation scheme involving a two-channel ADC architecture. The prototype ADC, fabricated in a 0.18 μm CMOS process, achieves 81dB SFDR at 0.9V and 2MSPS (12MHz clock) after calibration. The ADC operates up to 5MSPS (30MHz clock) with 4dB degradation. The total power consumption is 12mW, and the active die area is 1.4 mm².

I. INTRODUCTION

The continued down-scaling of power supply voltage in the state-of-the-art deep submicron CMOS technology brings many obstacles to high performance switched-capacitor (SC) circuit design. The main challenges are in the design of fast settling and high accuracy CMOS sampling switches, high gain opamps at ultra low supply voltage, and good signal-to-noise-ratio in the low signal swing system. Thus, in order to achieve high performance at reduced supply voltage, it is necessary to explore simple and efficient design techniques that can overcome or mitigate these issues.

This paper presents a prototype algorithmic ADC design which incorporates opamp-reset switching technique (ORST) [1]-[4] to achieve high speed operation at very low supply voltage. Because all nodes of ORST operates within the supply voltage rails, there is no added long-term reliability issues as in clock boosting and bootstrapping techniques [5][6][7]. This prototype ADC also incorporates a new background digital calibration which corrects the errors caused by finite opamp gain, capacitor mismatches, and incomplete linear settling [8]. The rest of this paper is organized as follows: Section II describes the proposed calibration scheme; Section III details circuit design; experimental results are summarized in section IV; and conclusions are given in section V.

II. BACKGROUND DIGITAL CALIBRATION USING CORRELATION

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In the circuit implementation of a multiplying digital-to-analog converter (MDAC), the non-ideal effects coming from capacitor mismatches and finite opamp gain will add errors to the conversion accuracy. Figure 1 shows a functional diagram of a 1.5-bit-per-stage pipeline ADC in the presence of these non-ideal terms, α_i , β_i and δ_i . The “capacitor-flip-over” MDAC structure is assumed in this functional diagram. Since signal-independent charge injection and opamp offset only add to the overall pipeline ADC offset, they are not shown in Fig. 1. The resulting analog output of an MDAC is

$$V_o = (1 + \delta)((2 + \alpha) \cdot V_i - D \cdot (1 + \beta) \cdot V_{ref})$$

where D is ± 1 or 0 depending on the input voltage level (i.e. the sub-ADC output). For a practical pipeline ADC, the conversion will be inaccurate due to these non-ideal terms and a calibration would be needed to achieve an improved performance.

One simple and robust calibration method is the equivalent radix calibration [9][4][8] which we have adopted for this implementation. In the radix-based calibration, the correct digital output of a non-ideal ADC can be calculated by applying the measured/extracted radix numbers (one per 1.5-bit MDAC stage) to the uncorrected digital code.

In pipelined ADCs which incorporate digital redundancy, there is an efficient way to do the background radix detection. We propose this method as illustrated in Fig. 2. A scaled (by approximately 1/8) binary pseudo-random noise sequence is injected at the input of the sub-ADC. The resulting ADC digital output D_o is

$$D_o = (V_i + Q_N + (1/8)P_N) \cdot ra_{es} - (Q_N + (1/8)P_N) \cdot ra + O_N$$

where P_N is the pseudo-random noise sequence, ra is the actual radix, ra_{es} is the estimate of the radix in digital domain, Q_N is the quantization noise of this stage, and O_N includes all other noise sources such as thermal noise and quantization noise of the back-end ADC.

If we correlate the ADC digital output D_o with the same pseudo-random sequence (see Fig. 2), and assuming a perfect correlation process, we get the radix error

$$e = (1/8)(ra_{es} - ra). \quad (1)$$

A near perfect correlation process can be assumed if the pseudo-random sequence is long enough, and the actual radix can be calculated by $ra = ra_{es} - 8e$.

At a glance, this radix detection scheme may seem similar to the interstage gain error calibration schemes proposed in [10][11]. The key modification here is to inject the pseudo-random sequence at the input of the sub-ADC instead of the sub-DAC. This change gives us many advantages. First, the injected pseudo-random noise can now be considered time-varying (but limited/bounded) comparator offsets, thus it can be absorbed and corrected by the digital redundancy of the pipeline ADC without any performance degradation. It does *not* require that the input signal magnitude be reduced when injecting the pseudo-random noise. Second, we do not need to face the complications of needing an accurate match of scaling (1/8 value) in the analog and digital domain. Third, in the circuit implementation, the injection of pseudo-random noise can be done by randomly varying the comparator threshold level (comparator dithering). There is no change to the MDAC, which is the most critical and sensitive block in the pipeline ADC design. As a result, we can expect faster operation and less noise coupling from this radix detection scheme.

Although the proposed correlation-based algorithm of Fig. 2 can be employed “as is” to extract the equivalent radix, the process would be slower and less accurate than the foreground algorithm in [4]. The main reason is the strong interference from the input signal to the ADC. Specifically, when we correlate the ADC’s digital output with the pseudo-random sequence to detect the radix error, the input signal is transformed into noise at the same time (because the input signal is uncorrelated to the pseudo-random sequence). This input signal transformed noise will interfere with the radix error detection, making it very slow to reach high accuracy.

In order to further improve the correlation efficiency of the proposed calibration scheme, which in current form faces a strong interference from the input signal, we propose a two-channel ADC architecture shown in Fig. 3. We place two identical ADCs in parallel to build a two-channel ADC. The two ADC channels are not time-interleaved. Instead, they take the same input signal but with opposite polarity. While the final ADC output is properly generated from the two parallel ADCs, the digital correlation/calibration path uses the opposite polarity to eliminate the signal to maximize correlation efficiency. While the channel mismatches can severely degrade the SNDR in *time-interleaved* two-channel ADCs, here they only mildly reduce the efficiency of the background radix extraction algorithm because of the incomplete cancelling of the ADC’s input signal in the correlation process. No tones will be produced because the operations of these two ADC channels are parallel and synchronized, not time-interleaved.

At first glance, it may seem that the two-channel ADC architecture will double the die area as well as power dissipation. But in reality, it just increases the die area taken up by the comparators and the digital calibration circuitry. In high accuracy switched-capacitor circuits, the die size is dominated by the total capacitor area, as the capacitor size is determined by the kT/C noise requirement. Given the same SNR requirement and the same input signal magnitude, we can reduce each ADC channel’s capacitor size by half, thus the total capacitor size of this proposed two-channel ADC is equal to the total capacitor size of a conventional single chan-

nel ADC. Although the resulting noise power would be four times higher in the proposed two-channel ADC, the equivalent input signal power is also four times higher since the equivalent input signal magnitude is doubled (we take both ADC channels’ digital output). The SNR does not change. The main die size overhead is due to the fact that the number of comparators and digital calibration hardware is doubled (the numbers of opamps is also doubled but each opamp is smaller) in the two-channel ADC architecture.

Also illustrated in Fig. 3 is the overall iterative calibration method used. To achieve a very robust operation, we iteratively extract the equivalent radix instead of using Eq. (1). The radix update equations are

$$\begin{aligned} ra_{es}^+[n+1] &= ra_{es}^+[n] - \Delta \cdot ((Do^+ + Do^-) \otimes P_{N1}) \\ ra_{es}^-[n+1] &= ra_{es}^-[n] - \Delta \cdot ((Do^+ + Do^-) \otimes P_{N2}) \end{aligned}$$

where ra_{es}^+ and ra_{es}^- are the estimated radices of P and N channel ADC stages, respectively; P_{N1} and P_{N2} are the two pseudo-random noise sequences used in radix extraction; n is the iteration index; and Δ is the step size. The main advantage of this iterative method is that the calibration of each stage is insensitive to the errors of its back-end ADC.

III. CIRCUIT DESIGN

A prototype two-channel algorithm ADC was designed in a 0.18 μ m CMOS technology. Each channel includes two stages (1.5bit/stage). It takes six clock cycles to process one sample and produce 12-bit output. In the following, the design of some critical building blocks are described.

Figure 4 shows the low-voltage MDAC based on ORST. The conventional floating CMOS switches in the signal path are eliminated. The sampling capacitor is discharged by the resetting opamps in the previous stage. Here, one drawback is that the capacitor-flip-over MDAC architecture can not be used. And the reference voltage has to be injected through a separate capacitor C_{ref} which is scaled down to 1/8 of the sampling capacitor C_s . Note that the effective reference voltages are scaled accordingly (single input signal range is from 225mV to 675mV) for $V_{REFP}=0.9V$ and $V_{REFN}=0$. This also enables the use of NMOS or PMOS switches ($V_{th} \approx 0.45V$). The virtual ground voltage level is set to 125mV which is also operable with an NMOS switch. Because it is very difficult to implement the fully-differential topology employing a traditional common-mode feedback circuit at the 0.9V operation, a pseudo-differential MDAC architecture is used, as shown in Fig. 4. The classic common-mode error amplification problem in pseudo-differential pipelined ADC is alleviated by adding extra cross-coupling positive feedback capacitors [3]. This makes the common-mode gain of MDAC equal to one while keeping the differential gain of two. Therefore, any common-mode error will not be amplified from stage to stage down the pipeline.

Any pipelined/algorithm ADC requires a front-end sample-and-hold function. A track-and-reset circuit equivalent to a floating switch is needed in the ORST or switched-opamp architectures. An active tack-and-reset circuit with excellent linearity was proposed to meet this requirement in [4]. For

low input frequency applications, however, a simple passive track-and-reset circuit shown in Fig. 5(a) can be used instead. It has the advantages of low noise, ultra-low power consumption and very small die area. Observing that there is an input signal leakage during the resetting phase since the input node is always connected to the sampling capacitor (this leakage directly causes signal distortion due to the nonlinear on-resistance of the resetting switch), a cascaded track-and-reset passive circuit shown in Fig. 5(b) is employed in this implementation. The second R-MOSFET network further suppresses the undesired nonlinear input signal leakage. This simple passive implementation can operate down to extreme low-voltage power supply conditions, and easily meet a very high linearity requirement. Figure 6 shows the comparator module used in this design. It has several parallel signal paths to accommodate the input signal, the reference/threshold voltage, dither signal (for calibration), and common mode voltage adjustment. The sizes of capacitors are scaled to reduce the spread ratio and to avoid large amplitude scaling of input signal due to the capacitive voltage division. Note that there is no floating switch in the signal paths to enable ultra-low voltage ORST-equivalent operation. Two resistors are inserted at the differential input path to reduce the kick-back noise seen by the MDAC input.

IV. EXPERIMENTAL RESULTS

The prototype ADC was fabricated in a $0.18\mu\text{m}$ CMOS process. The die photograph is shown in Fig. 7, where the active die area is 1.4 mm^2 . The total power consumption is 12mW at 0.9-V supply and 2MHz sampling frequency (12MHz clock frequency).

Figure 8 shows a typical measured frequency spectrum with 80kHz input and 12MHz clock (2MSPS). Before calibration, the measured SFDR, SNR, and SNDR were 48dB , 51dB , and 46dB , respectively. After calibration, the SFDR, SNR and SNDR are improved to 81dB , 55dB , and 55dB , respectively. The performance is maintained to Nyquist input.

Figure 10 shows the dynamic performance versus conversion rate (clock frequency is six times of conversion rate). The SFDR remains better than 80dB up to 3.2MSPS and degrades to 77dB at 5MSPS . After that, the SFDR drops quickly (limited by opamp slew rate). Figure 9 shows the dynamic performance versus power supply voltage. In the range of 0.9V to 1.3V power supply voltage, the dynamic performance is steady and slightly better at higher supply voltage because of larger headroom and signal swing.

V. CONCLUSIONS

The CMOS design of a 0.9V 2MSPS (12MHz clock) algorithmic ADC demonstrating 81dB SFDR was presented. The ADC operates up to 5MSPS (30MHz clock) with 4dB degradation. A passively cascaded track-and-reset circuit was employed to drive the first stage MDAC. The overall linearity of the ADC was greatly enhanced by applying a novel background digital calibration. An unprecedented combination of linearity and ultra low voltage operation for pipelined/algorithmic ADC was reported. The prototype IC was fabricated in a $0.18\mu\text{m}$ CMOS process, and the ADC occupying 1.4 mm^2 of active die area dissipates 12mW at 0.9V power supply.

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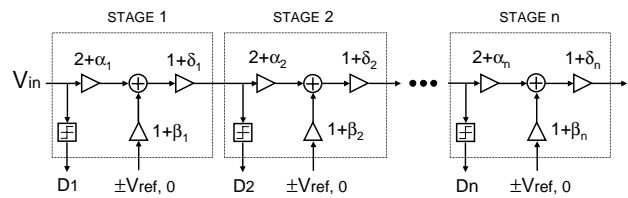


Fig. 1. Functional diagram of a pipeline ADC (1.5-bit-per-stage)

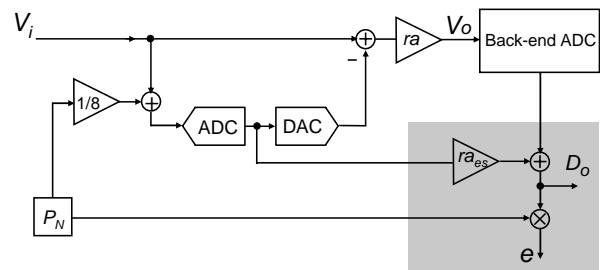


Fig. 2. Background equivalent radix extraction

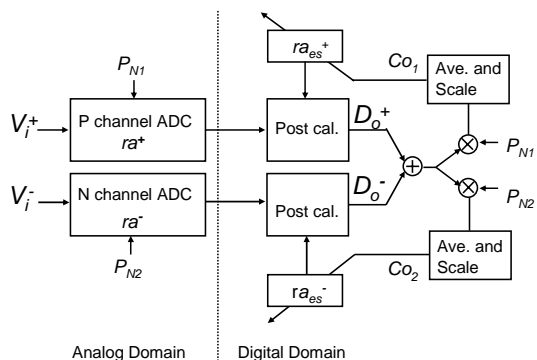


Fig. 3. Overall ADC with proposed background digital calibration

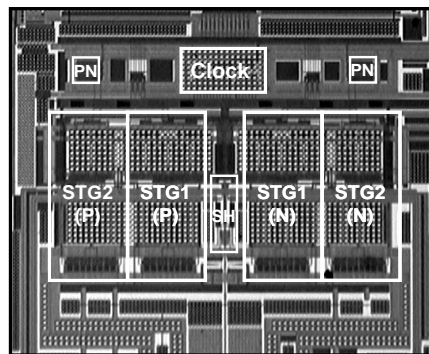


Fig. 7. Die photograph of the prototype ADC

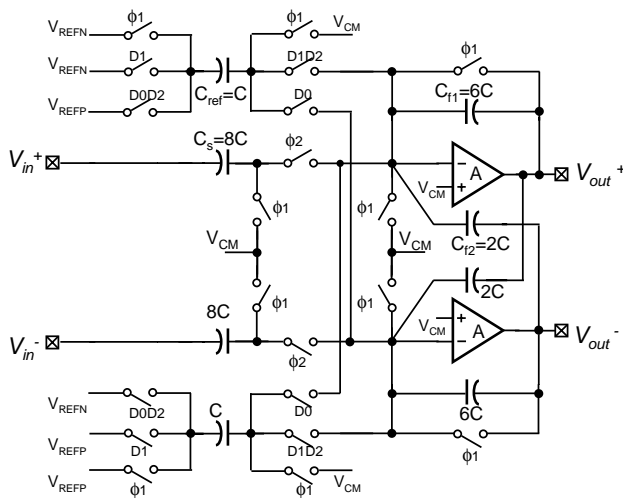


Fig. 4. Low-voltage MDAC

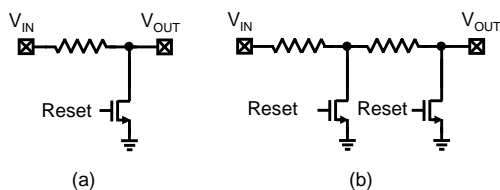


Fig. 5. Passive track-and-reset circuit MDAC

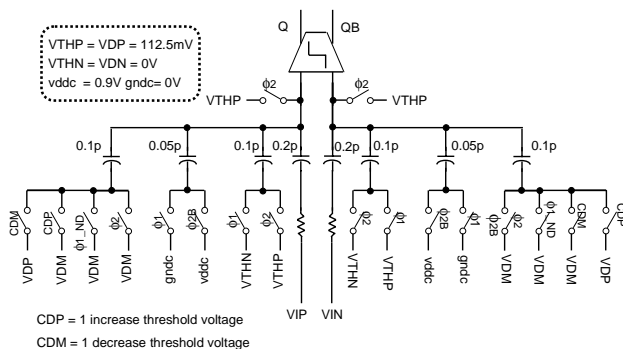


Fig. 6. Low-voltage SC comparator with dithering

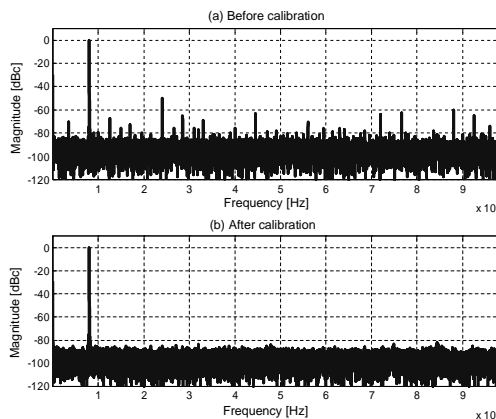


Fig. 8. Measured ADC output spectrum at 2MSPS

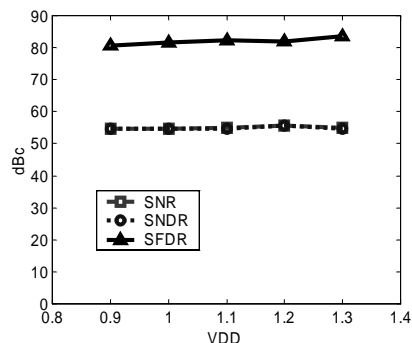


Fig. 9. Dynamic performance vs. power supply voltage

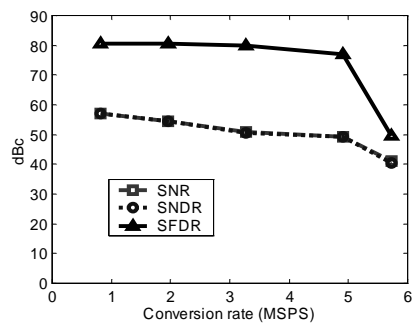


Fig. 10. Dynamic performance vs. conversion rate