A 10MS/s 11-b 0.19mm^2 Algorithmic ADC with Improved Clocking

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Abstract

A 10Ms/s 11-b algorithmic ADC with an active area of 0.19mm^2 is presented. Using an improved clocking scheme, this design overcomes the speed limit of algorithmic ADCs. The proposed ADC employs amplifier sharing, DC offset cancellation, and input memory effect suppression to reduce area and power, and achieve high linearity. The ADC implemented in a 0.13μm thick gate-oxide CMOS process achieves 69dB SFDR, 58dB SNR, and 56dB SNDR, while consuming 3.5mA from 3V supply.

Introduction

Pipelined analog-to-digital converters (ADCs) are used in medium to high speed applications such as video and communication systems. It is very beneficial to replace these pipelined ADCs with algorithmic data converters due to their well-known advantages such as low power and small chip area. However, algorithmic ADCs are inherently slower due to the cyclic nature of their conversion process. In a conventional algorithmic ADC with two multiplying digital to analog converters (MDACs), two bits are resolved each clock cycle - one bit in each phase - and hence the total conversion time for N-bit overall resolution is N/2-clock cycles. In this paper, we propose an improved clocking scheme that speeds-up the conversion rate of the algorithmic ADC with minimal area and power overhead. The proposed ADC employs op-amp sharing to further reduce power. Techniques to suppress memory effect and DC offset are presented.

Proposed Architecture

The block diagram of the proposed ADC is shown in Fig. 1. The fundamental idea behind the proposed architecture arises from the following observation. In a conventional algorithmic ADC, the conversion time for each bit is equal to the clock period irrespective of the weight of the resolved bit. In the proposed architecture, after the most significant bit (MSB) conversion takes place, the minimum clock period is determined to resolve each of the following least significant bits (LSBs). The accuracy requirement of the following conversion cycles is proportionally scaled and therefore the time for conversion can also be scaled. As shown at the bottom of Fig. 1, a delay locked loop (DLL) is used to synthesize an internal clock from an external clock. This internal clock relaxes MSB conversion time and progressively reduces the following bit conversion times. Note that unlike in a conventional algorithmic ADC, the external clock frequency is same as data conversion rate.

Amplifier sharing between the two MDACs of the algorithmic ADC reduces power consumption. However, amplifier sharing has two inherent drawbacks. First, since the input node of the amplifier is never reset, the current MDAC output depends on the previous residue, thus degrading the linearity of the overall converter. This is often referred to as *memory effect*. The memory effect between the last (LSB) conversion stage and the first (MSB) conversion stage is particularly detrimental. This memory effect is suppressed by resetting the amplifier input before sampling the ADC input. The timing for the reset signal (RS) is shown in Fig. 1. Second, amplifier sharing exacerbates the ADC offset since the amplifier is active in every clock phase and the amplifier DC offset has same polarity and amount in every conversion step. The feedback signal polarity inverting (FSPI) technique in [2] to reduce the DC offset is extended to an algorithmic ADC as shown in Fig. 2(a). While the original FSPI technique reduces the offset by one third, the improved FSPI eliminates the output referred offset. The measured output offset is within +2.5/-3.5 LSB as shown in Fig. 2(b).

Experimental Results

A measured SFDR vs. conversion rate is shown in Fig. 3. The SFDR with a conventional clock degrades with an increase in conversion rate while the proposed clocking scheme maintains almost the same SFDR from 9Ms/s to 16Ms/s conversion rate. Fig. 4 shows the measured DNL and INL, where the peak DNL is +0.85/-0.9LSB, and the peak INL is +3/-3.5LSB. The measured output spectrum with 1-MHz sine input signal and 10Ms/s conversion rate is shown in Fig. 5. The measured performance summary is presented in Table. 1. The chip micrograph is shown in Fig. 6.

Acknowledgments

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References

[1] M. Kim et al, "An improved algorithmic ADC clocking scheme," *in Proc. IEEE Int. Symp. Circuits and Systems*, vol. 1, pp. 549–592, May 2004.

[2] B. Min et al.,"A 69-mW 10-bit 80-MSample/s pipelined CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2031–2039, Dec 2003.

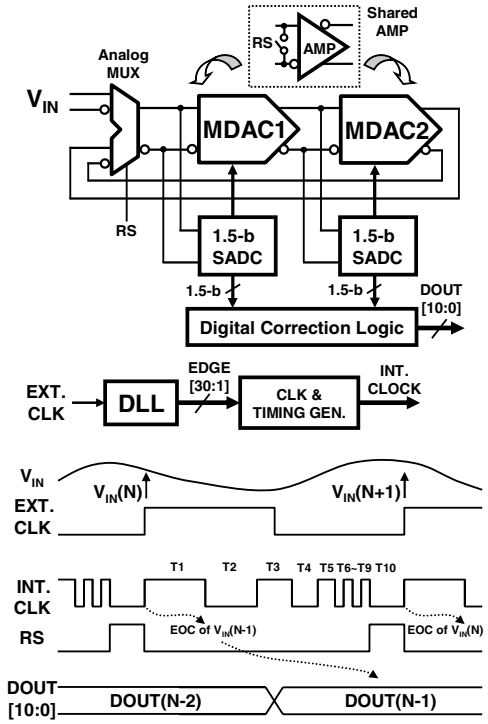

Figure 1: Block diagram of the proposed algorithmic ADC.

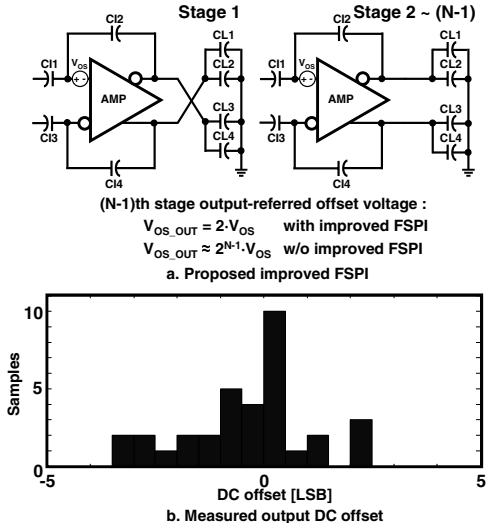

Figure 2: Improved FSPI technique and measured ADC output DC offset.

Table 1: Performance summary

Resolution	11-bit
Conversion Rate	10 MSPS
Technology	0.13 um Thick Gate-Oxide CMOS
Supply Voltage	3V
Power Consumption	ADC core : 10.5mW ,DLL : 4.5 mW
SFDR/SNR/SNDR	69dB / 58dB / 56dB
DNL/INL	0.9 LSB / 3.5 LSB
Active Die Area	ADC core : 0.19 mm^2 ,DLL : 0.05 mm^2

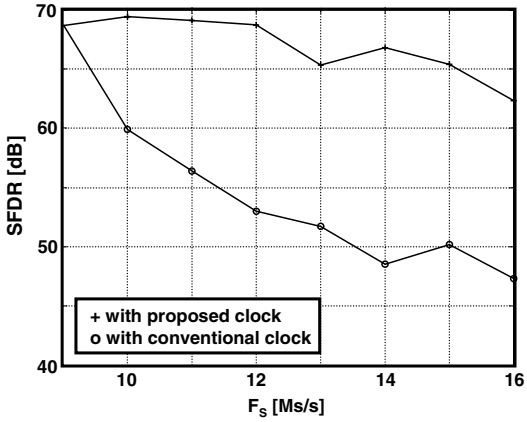

Figure 3: A measured SFDR vs. conversion rate plot.

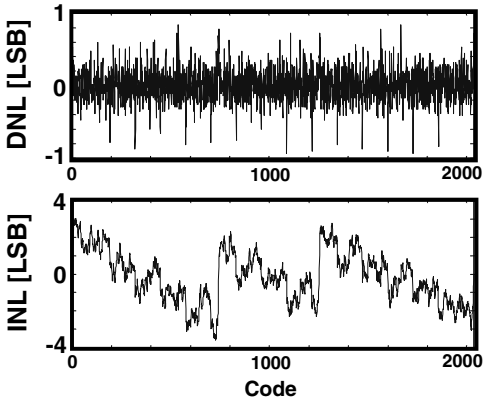

Figure 4: Measured nonlinearity.

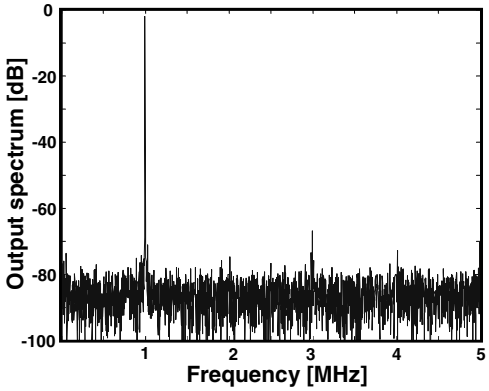

Figure 5: Measured output spectrum.

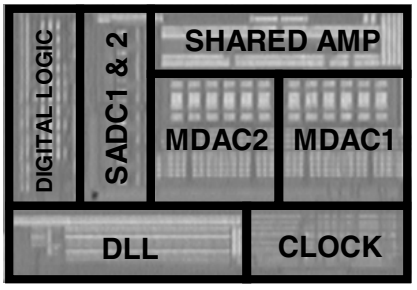

Figure 6: Chip micrograph.