An On-chip Calibration Technique for Reducing Supply Voltage Sensitivity in Ring Oscillators

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Abstract

A technique for reducing ring oscillator supply voltage sensitivity using on-chip calibration is described. A 1V 0.13µm CMOS PLL demonstrates robust performance against VCO supply noise over operating frequencies of 500MHz-2GHz. The measured rms jitter of the proposed PLL with on-chip calibration is 4.4ps for an operating frequency of 1.4GHz in the presence of 10mV 1MHz VCO supply noise, while a conventional VCO measures 19.4ps rms jitter. The total power consumption of the PLL is 9.4mW, and the core die area of the PLL with calibration circuitry is 0.064mm^2.

Introduction

Conventional methods employ voltage regulators to suppress supply voltage noise in ring oscillators at the cost of reduced voltage headroom. In the design of oscillators and PLLs at 1V supply, alternative techniques are preferred.

Many ring oscillator designs control PMOS transistor bias to tune the operating frequency. For example, in a Lee-Kim delay cell [1], the gates of two PMOS transistors are controlled. Although the V_{GS} of the PMOS transistors can be made more stable by connecting the loop filter at the control node to the supply (instead of ground), the V_{DS} of the PMOS transistors increases with an increase in the supply voltage, resulting in positive supply voltage sensitivity. Adding a compensation circuit with negative supply voltage sensitivity can reduce the total supply sensitivity [2]. However, it is practically impossible to achieve accurate compensation due to process variations and the dependence of this sensitivity on the oscillation frequency. To ensure optimum compensation, we propose a new on-chip calibration technique that requires measuring only the polarity of the supply voltage sensitivity. This implementation is much simpler than the use of an on-chip jitter measurement [3].

Calibration Technique and Circuits

A variable supply voltage is needed to measure the supply voltage sensitivity. As in Fig. 1(a), three PMOS transistors with different sizes are inserted in series between the VDD node and the supply node of the VCO. The three PMOS transistors in triode have nominal series resistance values of 18, 12, and 6 ohms. Different supply voltages V1, V2, or V3 can be achieved by turning on one of the transistors M1, M2, and M3. Fig. 1(b) summarizes the simulated voltage drops between VDD and the three possible supply voltages. The reductions in the voltage headroom are very small, and the series resistance provides a small amount of supply isolation.

A 4-stage ring oscillator with the compensation circuit is shown in Fig. 2. Based on a Lee-Kim delay cell, transistors Mn1 and Mn2 are added between the output nodes and ground. The gates of Mn1 and Mn2 are connected to the diode connected NMOS transistor M0 (node V_B). When the supply voltage is increased, V_B also increases, causing Mn1 and Mn2 to sink more current to ground. This mechanism slows the oscillator and thus creates a compensation for the VCO supply voltage sensitivity.

To provide optimum compensation for supply voltage sensitivity at all operating frequencies, the magnitude of the negative sensitivity of the compensation circuit needs to be controlled. This is shown in Fig. 3(a), where V1, V2, and V3 correspond to the supply voltages in Fig. 1. To tune the negative sensitivity, a digitally controlled current I_B is used to bias the transistor M0 in Fig. 2. When current I_B is increased, the voltage V_B is reduced, resulting in a reduced compensation of the supply sensitivity. The relationship between the overall supply voltage sensitivity $\partial f_{osc} / \partial V_{Supply}$ and the current I_B is shown in Fig. 3(b).

To effectively cancel the supply voltage sensitivity, current I_B should be calibrated. Only the sign of $\partial f_{osc} / \partial V_{Supply}$ is important. When this sensitivity measure is positive, the VCO runs faster under the higher supply voltage V3 than V1 ($f_{osc}|_{V3} > f_{osc}|_{V1}$), and I_B should be decreased. Conversely, when $f_{osc}|_{V3} < f_{osc}|_{V1}$, I_B should be increased. This trimming procedure should be continued until the equilibrium ($f_{osc}|_{V3} = f_{osc}|_{V1}$) is reached. When I_B is trimmed, the supply voltage V2 is used for the VCO. The V2 supply (between V1 and V3) yields a VCO supply voltage sensitivity that is closer to zero.

The schematic of the PLL which includes the calibration circuitry is shown in Fig. 4(a). Fig. 4(b) shows the timing diagram. The current I_B is controlled by a 5-bit word with 10µA LSB. These five bits are provided by a successive approximation register (SAR) ADC. The binary search algorithm has been implemented in the calibration scheme. The calibration procedure starts by "10000" reset, and the binary search algorithm completes in five calibration cycles. Each calibration cycle consists of lock-in and open-loop phases. To provide an open-loop, a CMOS switch is added between the charge-pump (CP) and the loop filter. The charge-injection of the switch is negligible, since the capacitance of the switch is much smaller than that of the loop filter.

In the lock-in phase, the supply voltage V3 is used for the VCO. The signal CLK_C is kept "1" for a time period of $2^6/f_{ref}$ to ensure the PLL settles, where f_{ref} is the reference clock frequency. In the following open-loop phase, the VCO supply voltage is changed to V1 and CLK_C breaks the loop. Because the control voltage (V_{ctrl}) does not change instantly, the free-running VCO oscillation frequency changes due to the change in the supply voltage. This frequency change can be observed at the output of the CP, causing the output V_{CP} to increase or decrease. The CP output is fed to two comparators. The voltage V_{CP} continues to either increase or decrease until it causes one output of the comparators to flip, which triggers an overflow signal to finish the open-loop phase. The open-loop phase also terminates if none of the comparators trigger within the time period of $2^6/f_{ref}$. At the end of the open-loop phase, the current bit of the SAR is determined and the next significant bit is preset to "1". This calibration cycle is repeated until all bits have been determined.

Test Chip and Measurements

The proposed PLL with the calibration circuitry has been fabricated in a 0.13µm CMOS process. A 4-stage ring VCO has been implemented. It incorporates dual-delay paths [4] to extend the frequency range for low supply voltage operation.

The SAR can be controlled manually for evaluation purposes. The measured rms jitter of the PLL versus 5-bit word control for I_B at 1.4GHz operation is shown in Fig. 5. The noisy supply voltage is a 10mV 1MHz sinusoidal signal added on top of the VCO supply. The measured performance is quite different depending upon the digital code. The code "11111" corresponds to a conventional VCO without the compensation circuit. The on-chip auto-calibration circuit converges to "01001". The measured rms jitter is improved from 19.4ps with the code "11111" to

4.4ps with "01001". The modified VCO consumes 5.2mA, and the other circuits in the PLL draw 4.2mA from the 1V supply. The PLL loop bandwidth is 2MHz. The proposed VCO with the help of the calibration circuits demonstrates robustness to supply noise over the full operating frequency range from 500MHz to 2GHz. The die photo of the test chip is shown in Fig. 6. The core areas of the PLL and the calibration circuitry are 0.051mm^2 (230µm×220µm) and 0.013mm^2 (160µm×80µm), respectively.

Conclusions

A ring-oscillator based PLL with on-chip calibration has enabled successful integration of a supply noise insensitive PLL. The 1V 0.13µm CMOS prototype IC measurement results have confirmed robust operation in the presence of VCO supply noise.

Acknowledgements

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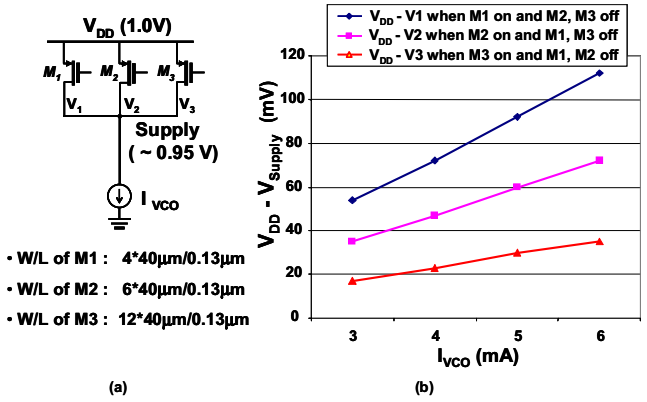

Fig. 1 (a) PMOS transistors are added to vary the supply voltage. (b) Comparison of simulated voltage drops with different settings.

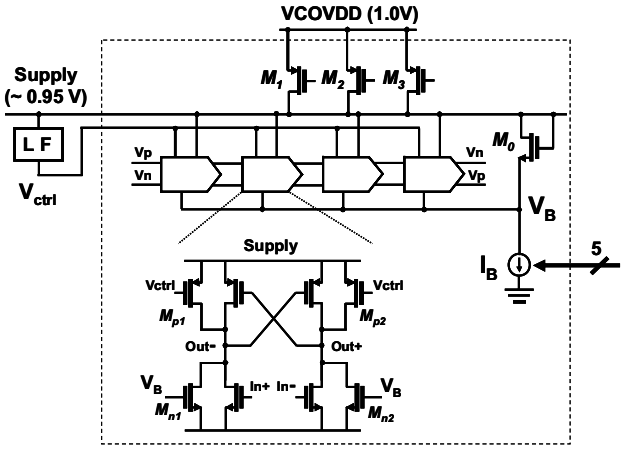

Fig. 2 A 4-stage ring oscillator with a new compensation circuit.

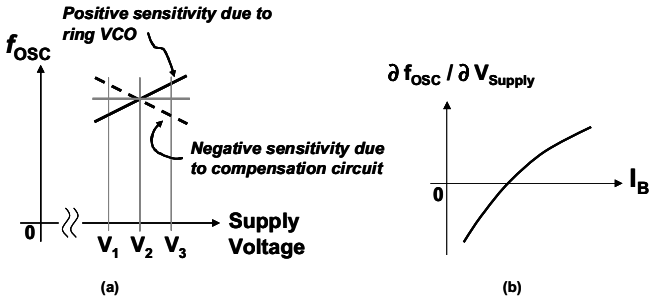

Fig. 3 (a) Optimal compensation for VCO supply voltage sensitivity. (b) Relationship between the supply voltage sensitivity and I_B.

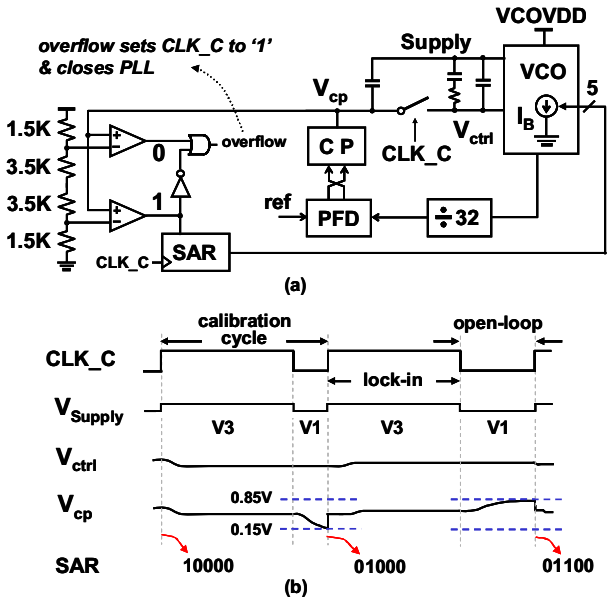

Fig. 4 (a) Schematic of PLL with calibration circuits. (b) Timing diagram.

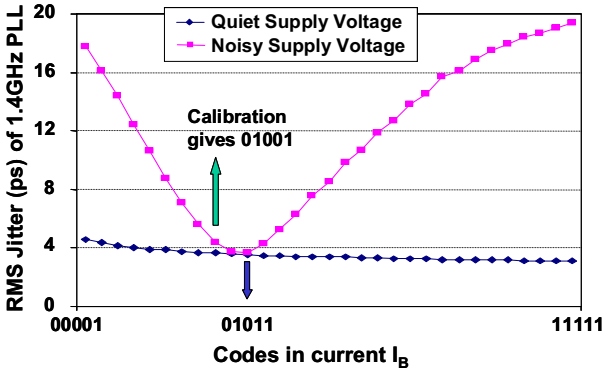

Fig. 5 Measured rms jitter of 1.4GHz PLL. The on-chip calibration provides nearly optimal performance.

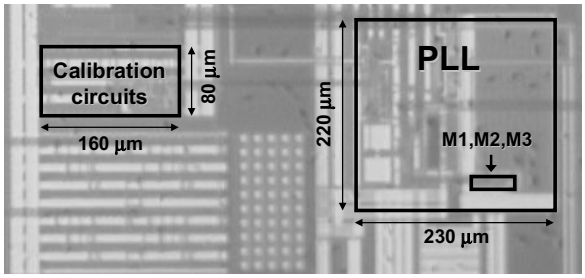

Fig. 6 Die photo.