# A 0.8V, 88dB Dual-Channel Audio $\Delta\Sigma$ DAC with Headphone Driver

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## Abstract

A 0.8V 3rd-order $\Delta\Sigma$ DAC with headphone driver is presented. The circuit requires only one opamp per channel, shared by the internal DAC, the FIR and 2nd-order Sallen-Key low-pass filter, as well as by the headphone driver. The prototype IC implemented in a 0.35$\mu$m CMOS process achieved 88dB dynamic range (DR), while consuming 2.6mW from a 0.8V supply.

## Introduction

Battery-powered portable audio devices require low-voltage, low-power, and medium-accuracy digital-to-analog converters (DACs). The proposed structure is inherently suitable for low-voltage and low-power applications. Fig. 1 shows the block diagram of the complete DAC system. The input of the DAC is a 16-bit serial digital signal DIN; the analog output AOUT drives the headphone load (16$\Omega$ parallel with 300pF).

## Interpolator and $\Delta\Sigma$ Modulator

The digital section of the DAC is implemented in a chip which includes the interpolation filter, the $\Delta\Sigma$ modulator and the dynamic element matching (DEM) circuitry. A hardware-efficient dual-channel interpolation filter is used. It contains three cascaded FIR half-band filters, followed by a sample-and-hold stage. It interpolates to an OSR of 64, and achieves 57dB stopband attenuation and $\pm$0.02dB passband ripple. The orders of the three FIR filters are 66, 14, and 2. A direct-form structure is selected for each FIR filter to minimize its hardware overhead. Each filter coefficient is quantized as a sum of a few powers of 2, and is realized as a series of shift and addition operations without any multiplier. The required accuracy for each filter coefficient was relaxed proportionately with its distance from the center tap, which allows extra hardware saving for each FIR filter. The data streams from the stages of the interpolation filters are time-interleaved appropriately between the two channels for proper dual-channel operation in a hardware-efficient manner. This required a doubled operating frequency and extra registers.

The main design goals for the $\Delta\Sigma$ modulator were: 1) reduced complexity of the reconstruction filter; 2) reduced sensitivity to clock jitter of the following analog circuitry; 3) reduced idle tones; 4) minimized wordlengths for the adders and registers. A third-order $\Delta\Sigma$ modulator with 7-level truncator, shown in Fig. 1, was adopted. The wordlengths in each accumulator were reduced by using a direct feedforward path with gain $b_2$ from the input to the quantizer. The local feedback path ($-g_1$) in the modulator loop minimizes the inband quantization noise by placing two zeros near the edge of the signal band. Data-weighted averaging (DWA) is applied for shaping the noise due to element mismatch in the following resistor-array DAC. The hardware requirement for dual-channel operation in the $\Delta\Sigma$ modulator and DWA was also minimized by sharing hardware between the two channels.

This work was supported by Asahi Kasei Microsystems, and partly by NSF CAREER CCR-0133530.

## DAC, Analog Low-Pass Filter, and Driver

Fig. 2 shows the analog section of the DAC, which includes a resistor-array DAC (R-DAC), a second-order Sallen-Key low-pass filter, and the headphone driver. In the resistor-array DAC, all switches are connected either to the high reference voltage ($V_{refh} = V_{dd}$) or to the ground. This avoids the problems with floating switches [1]. The opamp provides a virtual ground at nodes A and B for the DAC. Seven elements are used for the 7-level quantizer. This helps to suppress the spurs caused by DWA when the input signal is small. An analog first-order FIR filter is also integrated into this DAC ($d_i$ is delayed by one clock cycle with respect to $b_i$ in Fig. 2). This introduces a zero at one-half of the sampling frequency, and reduces the clock jitter sensitivity [2]. The embedded second-order IIR low-pass filter has a -3dB cutoff frequency at 150kHz, and its pole Q is 0.707. The values of all resistors and capacitors were optimized to achieve the minimum capacitor area for the given pole-Q, cutoff frequency, and the targeted SNR. Four extra R4 resistors were added (circled in Fig. 2) to make the output common-mode voltage $V_{dd}/2$. The opamp design is shown in Fig. 3. The output stage of the opamp incorporates a minimum current selector in the feedback loop, which contains the split output transistors of the first stage of the opamp. The loop regulates the bias current of the output transistors [3]. The loaded voltage gain of this opamp is 65dB; the UGBW is 7MHz.

## Experimental Results

The DAC was fabricated in Asahi Kasei Microsystem's 0.35$\mu$m CMOS technology, and occupies 1.6$\times$0.9 mm$^2$ and 1.6$\times$1.3 mm$^2$ active die area for the digital and the analog chip, respectively. Fig. 4 shows the measured overall output spectrum for a 1.17kHz, -60dB sine-wave input using a 0.8V power supply. There are no idle tones present in the quantization noise. The spurs caused by DWA rotation are also negligible (below -109dB). The SNDR versus input level from -85dB to 0dB (relative to 56% of the supply voltage) is shown in Fig. 5, for a supply voltage of 0.8V. The SNDR was measured over a 24kHz wide audio band. Without A-weighting, the prototype achieves 69dB peak SNDR and 88dB dynamic range with a 0.8V supply voltage. Using a 0.7V supply, the peak SNDR and the dynamic range are reduced to 68dB and 87dB, respectively. The chips consume 2.6mW power (2.5mW for the analog chip, 0.1mW for the digital chip) at 0.8V supply. The peak SNDR is limited by the second harmonic distortion

of the single-ended opamp for large input signal swings. The dynamic range and the peak SNDR gradually improve for supply voltages from 0.7V to 1.5V. The die photographs are shown in Fig. 6. The performance is summarized in Table 1.

## References


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[3] K. Langen and J. Huijsing, "Compact Low-Voltage Power-Efficient Operational Amplifier Cells for VLSI," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1482-1496, Oct. 1998.


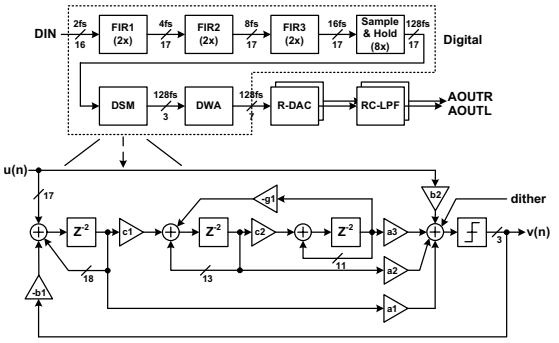


Figure 1: Dual-channel DAC and $\Delta\Sigma$ modulator.

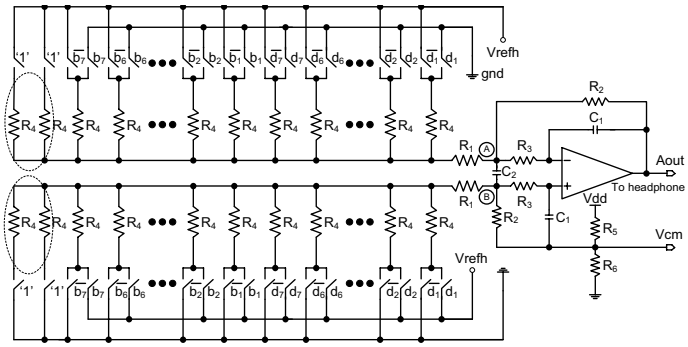


Figure 2: DAC combined with first-order FIR, second-order Sallen-Key filter, and headphone driver.

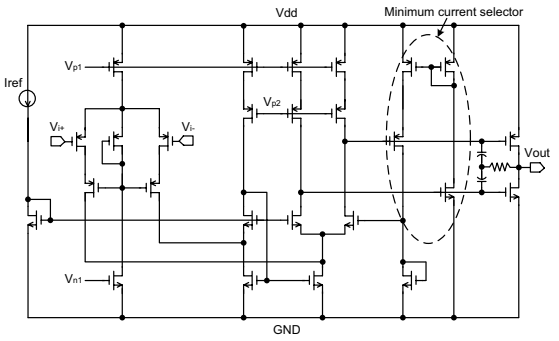


Figure 3: Opamp with class-AB output stage.

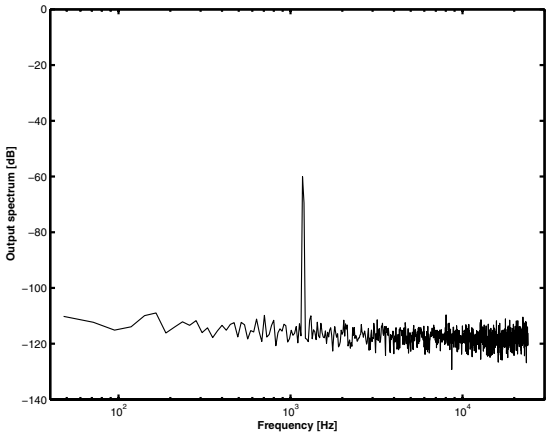


Figure 4: Measured output spectrum.

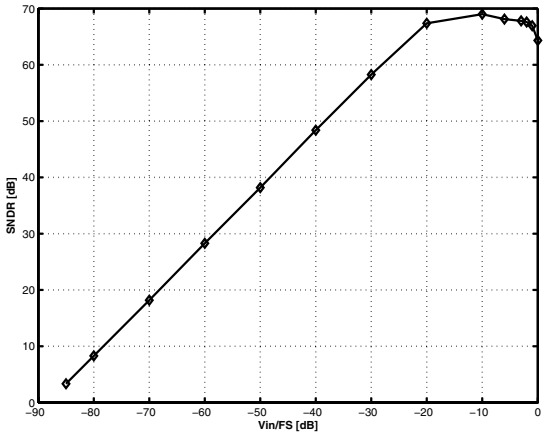


Figure 5: Measured SNDR.

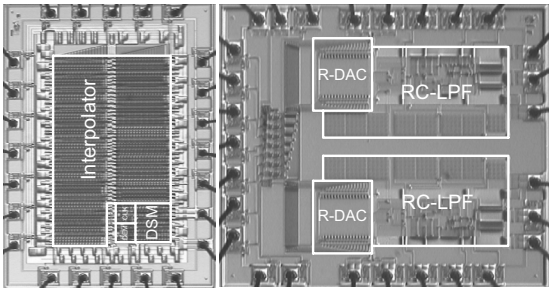


Figure 6: Die photographs.

Table 1: Performance summary.

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|---|---|
| Supply voltage | 0.8V |
| Signal bandwidth | 24kHz |
| Clock frequency | 3.072MHz |
| Oversampling ratio | 64 |
| Load | headphone (16Ω ∥ 300pF) |
| Power consumption | 2.6mW |
| Output range | $0.45V_{pp}$ (single-ended) |
| Peak SNDR | 69dB @ Vdd = 0.8V<br>68dB @ Vdd = 0.7V |
| Dynamic range | 88dB @ Vdd = 0.8V<br>87dB @ Vdd = 0.7V |
| Active die area | Digital chip: 1.6×0.9 mm$^2$<br>Analog chip: 1.6×1.3 mm$^2$ |
| Technology | 0.35$\mu$m CMOS |