A 0.9V 92dB Double-Sampled Switched-RC $\Delta\Sigma$ Audio ADC

Min Gyu Kim, Gil-Cho Ahn, Pavan Kumar Hanumolu, Sang-Hyeon Lee[1],
Sang-Ho Kim[1], Seung-Bin You[1], Jae-Whui Kim[1], Gabor C. Temes and Un-Ku Moon

School of the EECS, Oregon State University, Corvallis, OR 97331
[1]Samsung Electronics, Yongin, Korea

Abstract

A 0.9V third-order 1.5bit delta-sigma ADC with simple dynamic element matching (DEM) is presented. A fully-differential low-voltage double-sampling structure avoids use of clock boosting or bootstrapping. It operates from 0.65V to 1.5V supply with minimal performance degradation. The prototype IC implemented in a 0.13μm CMOS process achieves 92dB DR, 91dB SNR and 89dB SNDR, while consuming 1.5mW from a 0.9V supply.

Introduction

The demand for portable multimedia systems and the continued down-scaling of device dimensions resulted in rapid improvement in the performance of integrated systems. In order to reduce power consumption and the electric fields that accompany device scaling, it is necessary for circuits to operate from reduced supply voltages. A reduced supply voltage results in significant power savings in digital circuits. However, the power consumed in analog circuits is likely to increase because the reduced supply voltage limits the analog signal power and mandates lower noise. For this reason, high-performance ADCs should operate with a low voltage supply, and also have low power consumption. Double-sampling scheme (DSS) is one possible solution for reducing power consumption. However, it requires complex bootstrapping schemes in low-voltage systems. This paper presents a high-performance low-voltage double-sampling audio ADC. The switched-RC (SRC) [1] technique is incorporated in order to avoid clock-bootstrapping.

Proposed Architecture

Single-loop delta-sigma topology offers several advantages for low-power low-voltage operation, such as insensitivity to circuit non-idealities and simple circuitry. However, this topology requires a higher order for a given oversampling ratio (OSR) to achieve high signal-to-quantization noise ratio (SQNR). System-level simulations indicate that a third-order 1.5-bit (3-level) single-loop topology with double-sampling offers the best tradeoff between the required clock frequency, amplifier bandwidth and signal-to-noise ratio (SNR) for an audio ADC. The block diagram of the single-loop third order delta-sigma ADC with a 1.5-bit quantizer is shown in Fig. 1. The 1.5-bit quantizer allows the use of a simple DEM scheme suitable for low-voltage operation. In this scheme, the two 1-bit DAC elements are interchanged whenever the delta-sigma ADC output equals the middle code. One major disadvantage of the conventional DSS is noise folding due to path gain mismatch. The gain mismatch in the forward signal path does not degrade performance significantly. However, in the feedback path, it degrades the SNR due to noise folding into the signal band. The integrator circuit used in this design is shown in Fig. 2. The DSS using switched-RC branches is employed in the forward signal path, while fully-floating switched-capacitor branches [2] that are insensitive to gain mismatch are utilized in both the first and second feedback paths. A conventional DSS is used in the third integrator feedback path because the use of conventional double sampling scheme eliminates the stability issues caused by the additional pole introduced in the fully-floating switched capacitor configuration. The DSS SRC circuit not only doubles the OSR, but also overcomes some drawbacks of the SRC. The double sampling with the SRC allows a constant input resistance of the delta-sigma ADC, and the same opamp DC gain during both clock phases. The DSS also obviates the need for half-delay elements [1], because a half-period delay translates into a full period delay for the DSS.

Circuit Design

Pseudo-differential opamps are frequently used in low-voltage applications to overcome the difficulty of realizing the low-voltage common-mode feedback (CMFB) required for a fully differential structure. The pseudo-differential configuration, however, suffers from several drawbacks, including increased noise, higher power consumption, larger area, and reduced PSRR/CMRR. In order to avoid these issues, a fully-differential amplifier with a low-voltage CMFB was employed. The amplifier consists of a folded-cascode first stage for low input common-mode voltage, and a common-source second stage for wide output swing. As shown in Fig. 2, an additional current source is used to shift the output common-mode level to be within the input common-mode range of the folded-cascode single-stage CMFB amp. Fig. 3 illustrates the circuit diagram of the low-voltage DSS comparator used in the 1.5-bit quantizer. It consists of a split-SRC input sampling network, a preamplifier A1 and a level-shifting amplifier A2 along with the two comparator latches L1 and L2. The decision levels are set by appropriately scaled capacitors C1 and C2, and the offset is canceled at the output of the preamplifier A1. The input common-mode level of A2 can be set as low as ground potential. This comparator can be used to realize a low-voltage multi-level quantizer, without needing floating switches.

Experimental Results

The ADC was fabricated in a 0.13μm CMOS technology. The measured output spectrum is shown in Fig. 4. The measured SNDR versus input signal level characteristic is shown in Fig. 5. The ADC can operate with supply voltages from 0.65V

to 1.5V with minimal performance degradation. The measured performance summary is presented in Table. 1. The chip micrograph is shown in Fig. 6.

Acknowledgments

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References

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[2] D. Senderowicz et al.,"Low-voltage double-sampled delta-sigma converters," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1907–1919, Dec 1997.

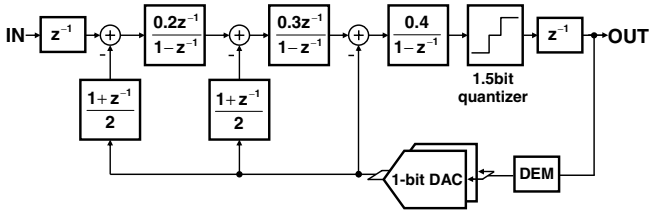

Figure 1: A third-order double-sampled delta-sigma ADC.

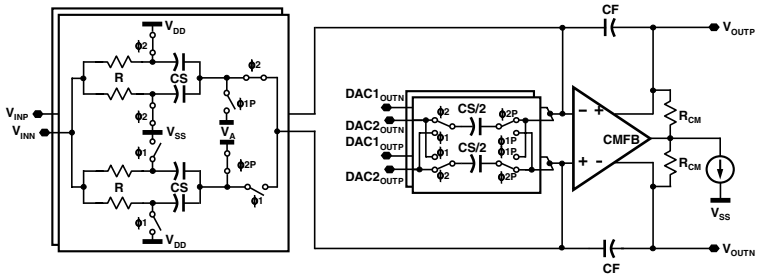

Figure 2: Low-voltage double-sampled integrator.

Table 1: Performance summary

Power supply voltage	0.65 V	0.9 V
Power consumption	1.1 mW	1.5 mW
Input range	0.87 V_{PP} (diff.)	1.1 V_{PP} (diff.)
Peak SNR	83 dB	91 dB
Peak SNDR	79 dB	89 dB
Dynamic range	87 dB	92 dB
Signal bandwidth	24 kHz	
Sampling frequency	6.144 MHz	
Clock frequency	3.072 MHz	
Oversampling ratio	128	
Active die area	1.6 X 0.9 mm^2	
Technology	0.13µm CMOS	

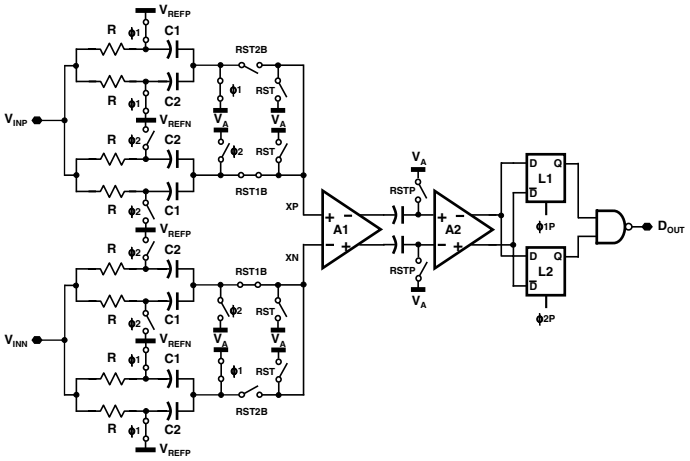

Figure 3: Low-voltage double-sampled comparator.

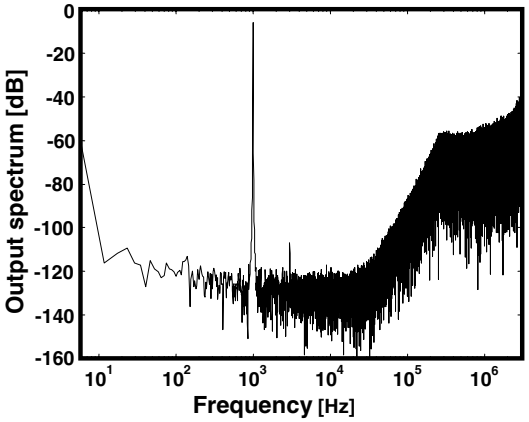

Figure 4: Measured output spectrum.

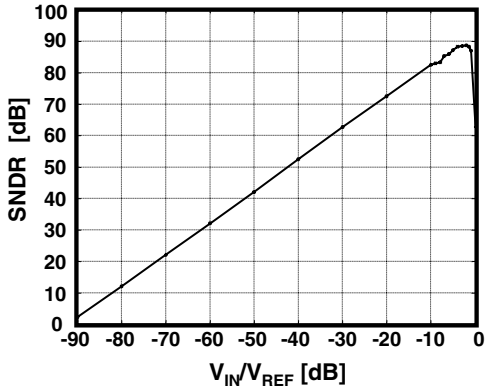

Figure 5: SNDR vs. input level for a 0.9 V supply voltage.

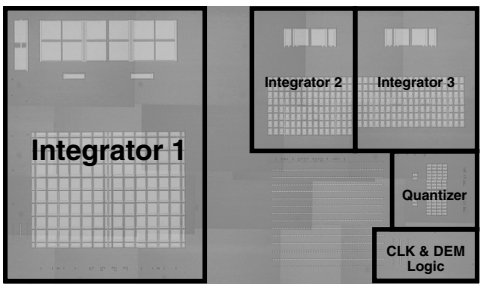

Figure 6: Chip micrograph.