A 12b 10MS/s Pipelined ADC Using Reference Scaling

G. Ahn, P. K. Hanumolu, M. Kim, S. Takeuchi[1], T. Sugimoto[1],
K. Hamashita[1], K. Takasuka[1], G. Temes and U. Moon

School of EECS, Oregon State University, Corvallis, OR

[1]Asahi Kasei Microsystems, Atsugi, Japan

Abstract

A 12b 10MS/s pipelined ADC using reference scaling achieves 62 dB SNDR and 72 dB SFDR for a 1MHz input. The prototype IC fabricated in a 0.35μm CMOS process employs interstage amplifiers with 45dB open-loop gain and consumes 19mW from a 2.4V supply.

Introduction

The demand for portable applications such as wireless communications and multimedia consumer electronics, combined with the growing trend of performing all signal processing in the digital domain, created a need for high-resolution analog-to-digital converters (ADCs). At the same time, the need for low power consumption becomes more important to achieve longer battery life. Pipelined ADC architecture offers excellent trade-off between speed and power, and is therefore a popular choice for implementing wireless and video front-ends. In the traditional pipelined ADC design, high DC gain amplifier is required to achieve accurate closed loop gain of the inter-stage multiplying digital-to-analog converter (MDAC). Multi-stage topology [1][2] or gain boosting [3] are the best-known techniques to achieve high amplifier gain. However, both these methods require large power consumption, and their performance is ultimately limited by the gain-bandwidth product of the process. In this paper, a new architecture is proposed to implement high-resolution ADC with a low-gain amplifier. To verify the proposed architecture, a 12b 10MS/s pipelined ADC was implemented.

Proposed Architecture

The pipelined ADC architecture employing the proposed reference scaling technique is shown in Fig. 1. It consists of a 2.5-bit first stage followed by eight 1.5-bit stages and is terminated by a 2-bit flash ADC. Similar to a conventional pipelined ADC, each stage resolves a fixed number of bits depending on the stage resolution, and passes on the amplified quantization error (residue) to the following stage**.** The linearity of this pipelined architecture is limited by the transfer gain accuracy of each stage. Inter-stage gain error during the residue amplification phase causes nonlinear transfer characteristics for the over-all ADC. In the proposed architecture, the reference voltage is also propagated through the same stages to introduce the same gain error as the residue.

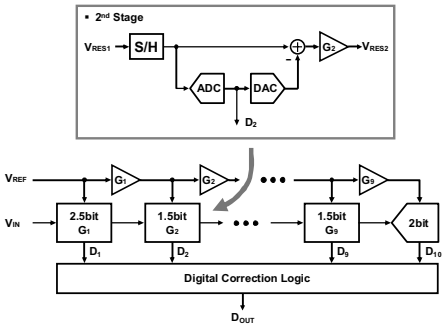

Fig. 1 Block diagram of the proposed ADC architecture.

By applying the same gain to both reference and signal, the interstage gain error is cancelled.

The two main sources of inter-stage gain error are capacitor mismatch and finite opamp gain. Since modern fine-line CMOS processes provide accurate matching up to 14 bits [1], only the gain error caused by low opamp gain is addressed in this design. The fundamental idea behind the proposed architecture arises from the following observation. In a conventional MDAC, the transfer gain accuracy is proportional to the opamp gain. So by introducing the same gain error into the reference voltage, the distortion caused by the finite opamp gain can ideally be cancelled. As shown in Fig. 2, the gain error is introduced into the reference by utilizing an additional capacitor array and sharing the same opamp. During the residue amplification phase of the first stage, the capacitor array of C_{R1}s samples the reference input V_{REF}. At the same time, the following stage MDAC and the comparator sample the residue output onto capacitors C_{S2} and C_{L2} respectively. During the following phase, the sampled reference is amplified by the same opamp and feedback factor, to reproduce the same transfer gain error. This *scaled* reference is then fed to the following MDAC stage. Note that this technique enables the use of MDAC with a low-gain amplifier for building a high resolution ADC, as long as the gain of the amplifier is the same during both phases. As a result of this relaxed gain requirement, a simple single stage amplifier with an open loop gain of 45dB was employed in this design.

Memory Effect and Offset Issue

One of the critical issues of the switched-capacitor circuit using low-gain amplifier is the memory effect. The stored charge on the parasitic capacitor of the virtual ground node

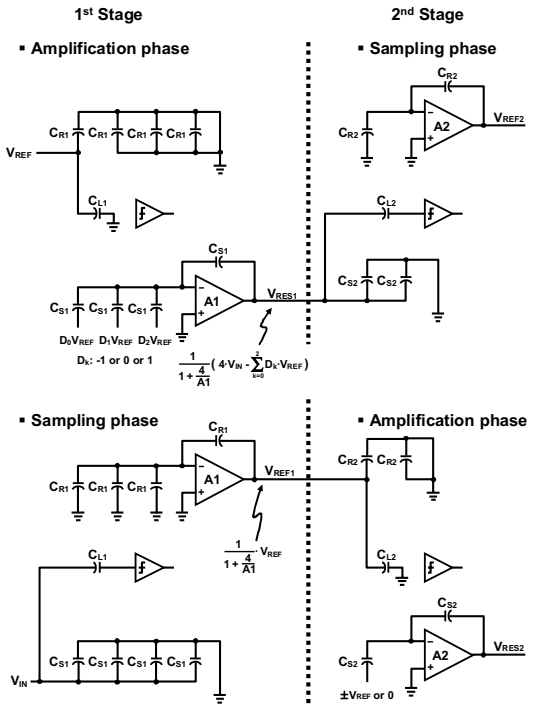

Fig. 2 MDAC with proposed reference-scaling technique.

varies with the output signal, and causes harmonic distortion. To reduce this distortion, the input and the output terminals of the amplifier are reset between the two clock phases.

In the conventional pipelined architecture, the effect of amplifier offset in the MDAC is mitigated by employing digital redundancy. However, in the proposed reference scaling scheme, the offset voltage of the opamp is amplified during the reference amplifying phase, and manifests itself as inter-stage gain error. To reduce this gain error, the offset of the first MDAC stage was cancelled, by trimming the output current of the amplifier. However, measured results indicate that the linearity of the ADC can be further improved by canceling the amplifier offset in the second and third stages as well.

Experimental Results

The prototype 12-bit pipelined ADC was fabricated in 0.35µm CMOS technology, and occupies 2.2×2.4 mm^2 active die area. Fig. 3 shows the measured nonlinearity of the ADC and the power spectrum of the output for a 1MHz, 1.1V peak-to-peak differential sine wave input using a 10MHz sampling frequency. The DNL is +0.52/-0.7 LSB, and the INL is +2.3/-3.1 LSB. The achieved SNDR is 62dB, and the SFDR is 72dB. For a 5MHz input sine wave, the SNDR and SFDR reduces to 57dB and 68dB. The power consumption with 2.4V supply is 14mW for the analog section, and 5mW for comparators and the digital section. The performance is summarized in Table I and the die photograph is shown in Fig. 4.

Acknowledgements

This work was supported by Asahi Kasei Microsystems, and partly by NSF CAREER CCR-0133530.

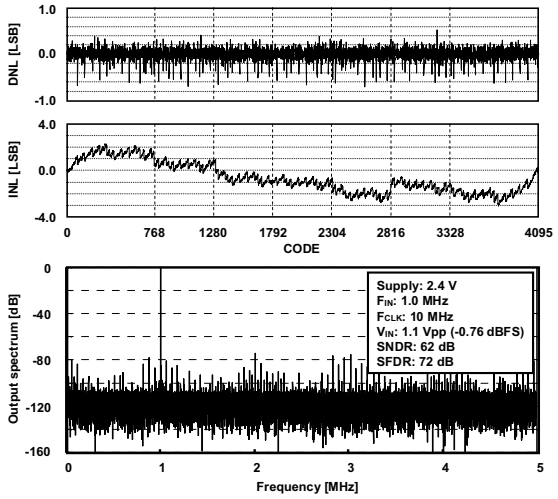

Fig. 3 Measured DNL, INL and output spectrum.

TABLE I
Performance summary

Power supply voltage	2.4 V
Resolution	12 bit
Sampling frequency	10 MHz
Input range	2.4 Vpp (differential)
DNL	< 0.7 LSB
INL	< 3.1 LSB
SNDR	62 dB @ FIN = 1 MHz 57 dB @ FIN = 5 MHz
Total power consumption	19 mW (including digital and I/O)
Active die area	2.2 X 2.4 mm^2
Technology	0.35 µm CMOS

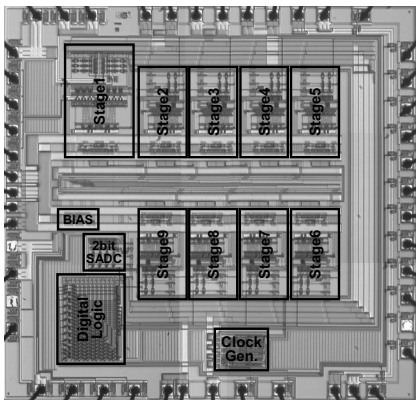

Fig. 4 Die photograph.

References

[1] W. Yang, D. Kelly, I. Mehr, M. T. Sayuk, and L. Singer, "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1931–1936, Dec. 2001.

[2] E. Siragusa and I. Galton, "A digitally enhanced 1.8-V 15-bit 40-MSample/s CMOS pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2126–2138, Dec. 2004.

[3] Y. Chiu, P. Gray and B. Nikolić, "A 14-b 12-MS/s CMOS pipeline ADC with over 100-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2139–2151, Dec. 2004.