ECE 272: Digital Logic Design Laboratory
Spring 2019

1 Course Information

Instructor: Matthew Shuman  
shuman@eecs.oregonstate.edu
Lab Website: http://eecs.oregonstate.edu/tekbots/courses/ece272

Lab times and TA office hours are posted on the lab website. Please check Canvas and your email regularly for course announcements.

This is a one-credit laboratory course meant to complement the material seen in ECE 271. It consists of 6 lab sections

2 Assignments & Grading

Your final grade in this course is made up of four parts: lab check offs, and lab reports. All written work is submitted on Canvas. You may work in pairs to complete your physical lab project (lab check off), but all written work (lab reports and pre-labs) must be completed individually. Any grade disputes must be brought to your lab Grading TA no later than a week after the grade is given. These are weighted and graded as follows:

2.1 Pre-Labs (20%)

Sections 3, 4, 5, and 6 have a pre-lab. Completing the labs in the allocated number of weeks is manageable if you do the required research before coming to lab. These assignments are worth 10 points each and are due before the beginning of the lab. Pre-labs CAN NOT be turned in late!

2.2 Lab Check Off (40%)

Each lab check off is worth 10 points per week (i.e. Section 1 is a one-week lab and is worth 10 points but section 6 is a two-week lab and is worth 20 points). Labs are checked off at the beginning of class one week after each lab. Late labs are not accepted.

2.3 Lab Report (40%)

Each lab report is worth 20 points. Please follow the template provided on Canvas. Note: This template is to give an idea of formatting. You should not copy any text or diagrams from the template. Lab reports are due on Canvas at the beginning of class one week after the end of each lab.

Late Reports: Reports may be turned in up to one week past the deadline at a 10 point deduction except for the last report of the term, which must be turned in on time. Reports are not accepted more than a week after the deadline. If there are special circumstance that will prevent you from completing your report on time, you should contact your grading TA as soon as possible.

2.4 Final Grades

Final course grades are assigned based on your final percentage as follows:
A  92.50 and up  
A-  89.50 to 92.49  
B+  86.50 to 89.49  
B  82.50 to 86.49  
B-  79.50 to 82.49  
C+  76.50 to 79.49  
C  72.50 to 76.49  
C-  69.50 to 72.49  
D+  66.50 to 69.49  
D  62.50 to 66.49  
D-  59.50 to 62.49  
F  less than 59.50

3  Lab Policies

Academic Dishonesty: You may work in pairs to complete the physical lab project (lab check off). All written work (pre-labs, lab reports, and peer reviews) must be completed individually. Turning in the same work as another student is plagiarism and will result in a zero for the assignment on the first offense. Subsequent offenses will be reported for academic dishonesty.

Citations: Any outside information must be cited in your assignments. Failure to do so will result in a 1 point deduction.

4  Term Schedule

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<thead>
<tr>
<th>Week</th>
<th>Section Title</th>
<th>Items Due</th>
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| 1    | Preface - Install Toolchain and Lab Etiquette  
Section 1 - Basic Combinational Logic and the DE10-Lite | None                             |
| 2    | Section 2 - Adders on an FPGA                                                 | Section 1 Check Off  
Section 1 Lab Report               |
| 3    | Section 3 - Combinational Logic (Seven Segment Driver)                        | Section 2 Check Off  
Section 2 Lab Report  
Section 3 Pre-Lab                  |
| 4    | Section 3 - Combinational Logic (Seven Segment Driver)                        | None                             |
| 5    | Section 4- Counters                                                           | Section 3 Check Off  
Section 3 Lab Report  
Section 4 Pre-Lab                  |
| 6    | Section 4- Counters                                                           | None                             |
| 7    | Section 5 - System Verilog                                                    | Section 4 Check Off  
Section 4 Lab Report  
Section 5 Pre-Lab                  |
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<th>Section 5 - System Verilog</th>
<th>Section 6- Video Graphics Array (VGA)</th>
<th>Section 5 Check Off</th>
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